CMOS PROGRAMMABLE PERIPHERAL INTERFACE

TMP82C55AP-2/TMP82C55AM-2
TMP82C55AP-10/TMP82C55AM-10

1. GENERAL DESCRIPTION AND FEATURES

The TMP82C55A (hereinafter referred to as PPI) is a CMOS high Speed programmable input/output interface with three 8-bit I/O ports. 24 I/O Ports are divided into two groups (Port A and Port B) which are programmable independently by control words provided by MPU. The PPI has three operation modes (Mode 0, 1 and 2) and is copable of versatile interface between MPU and peripheral devices.

The TMP82C55A is fabricated using Toshiba's CMOS Silicon Gate Technology.

(1) High Speed Version (TRD = 100ns MAX: TMP82C55AP-10/AM-10)

(2) Low power consumption
2mA Type.
10μA Max. (@5V, Stand-by)

(3) 5V ±10% Single power supply

(4) 24 programmable I/O ports

(5) Three operation modes (Mode 0, Mode 1, Mode 2)

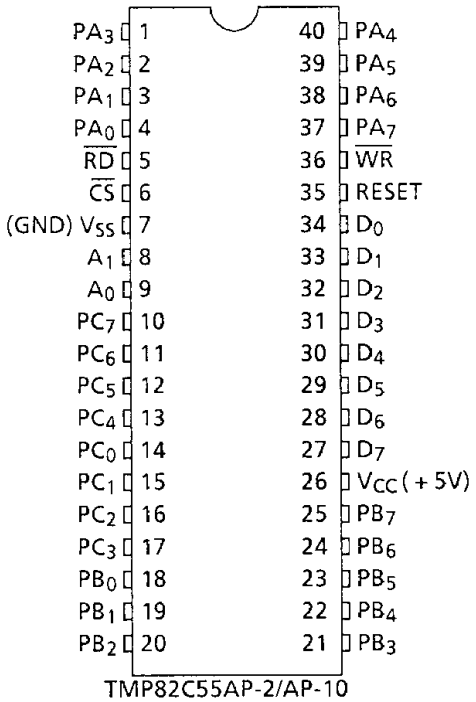
(6) Bit set/reset capability

(7) Up to 8 output ports of port B and C are capable of driving a darlington transistor (Min. −1.0mA @VOH = 1.5V)

(8) Extended operating temperature: −40 °C to +85 °C

(9) Available 40pin Standard DIP and SOP

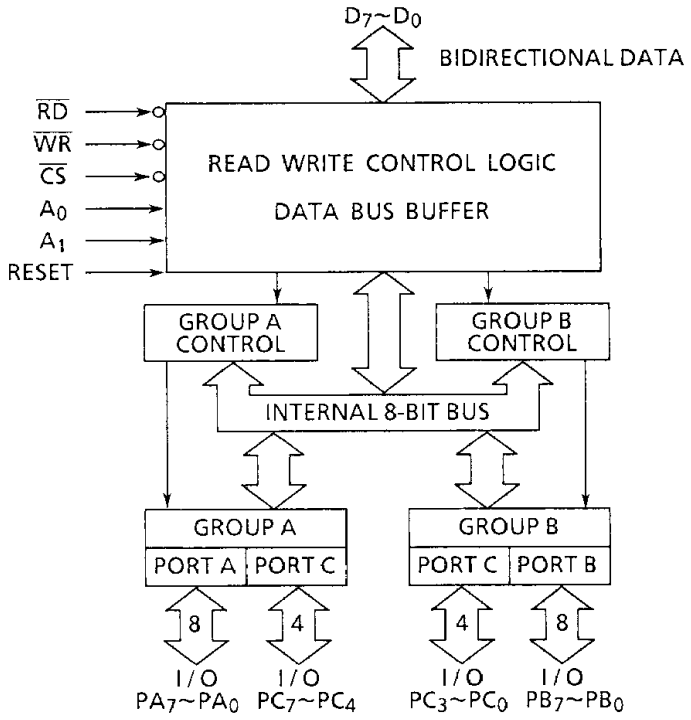
2. PIN CONNECTIONS (TOP VIEW)



TMP82C55AP-2/AP-10
TMP82C55AM-2/AM-10

050489

3. BLOCK DIAGRAM



050489

4. PIN NAMES AND PIN FUNCTIONS

Pin Name	Number of Pin	Input/Output 3-state	Function
D_0~D_7	8	I/O 3-state	3-state bidirectional 8-bit data bus. Used for data transfer with MPU. Also, used for transfer of control words to PPI and status information from PPI.
PA_0~PA_7	8	I/O 3-state	3-state 8-bit I/O Port A. Operation mode and input/output configuration are defined by software. Port A contains the output latch buffer and input latch.
PB_0~PB_7	8	I/O 3-state	3-state 8-bit I/O Port B. Operation mode and input/output configuration are defined by software. Port B contains the output latch buffer and input latch.
PC_0~PC_7	8	I/O 3-state	3-state 8-bit I/O Port C. Operation mode and input/output configuration are defined by software. Port C can be divided into two 4-bit ports by the mode control and also, used as the control signal for Port A and Port B. In this case, 3 bits of PC_0 to PC_2 are used for Port B and 5 bits of PC_3 to PC_7 for Port A.
$\overline{CS}$	1	Input	Chip select input. When this terminal is at "L" level, data transfer PPI and MPU becomes possible. At "H" level, the data bus is placed in the high impedance state and control from the processor is ignored.
$\overline{RD}$	1	Input	Read signal. When this terminal is at "L" level, data that is input into the port is transferred to MPU.
$\overline{WR}$	1	Input	Write signal. When this terminal is at "L" level, data or control word is written into PPI from MPU.
A_0, A_1	2	Input	Used for selecting Port A, B, C and the control registers. Normally, this terminal is connected to low order 2 bits of the address bus.
RESET	1	Input	When this terminals is at "H" level, all internal registers including the control register are cleared. In addition, all ports (Port A, B, C) are placed in the input mode (high impedance) of mode 0.
V_{CC}	1	Power Supply	5V
V_{SS}	1	Power Supply	GND

050489

5. FUNCTIONAL DESCRIPTION

The PPI is a programmable peripheral interface device with three 8-bit ports (Port A, B and C) and two control registers. 24 I/O ports are divided into 12-bit group A and group B. Group A consists of Port A and high order 4 bits of Port C, while Group B consists of Port B and low order 4 bits of Port C. Each group is independently programmable by control words provided from MPU. There are three operation modes available for the PPI. In mode 0, two 8-bit I/O ports and two 4-bit I/O ports can be programmed as input or output ports, respectively. In mode 1, 24 I/O ports are divided into Group A and Group B. 8 bits of each group are used as input or output port and of the remaining 4 bits, 3 bits are used as handshaking and interrupt control signal. Mode 2 is applicable only to group A and the ports are used as a bidirectional 8-bit data bus and 5-bit control signal. In case of Port C being used as the output, any bits of Port C can be set/reset.

There are two control registers; one is used for mode setting and the other for bit set/reset control. The control registers can only be written into. Further, when the reset input (RESET) becomes "1", the control registers are reset and all I/O ports are placed in input mode (high impedance status).

Table 5.1 Basic Operation of TMP82C55A

A_1	A_0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Function
0	0	0	0	1	Data bus ← Port A
0	1	0	0	1	Data bus ← Port B
1	0	0	0	1	Data bus ← Port C
0	0	0	1	0	Port A ← Data bus
0	1	0	1	0	Port B ← Data bus
1	0	0	1	0	Port C ← Data bus
1	1	0	1	0	Control register ← Data bus
×	×	1	×	×	Data bus = 3-state
×	×	0	1	1	Data bus = 3-state
1	1	0	0	1	inhibition of combination

050489

5.1 MODE SELECTION

There are three basic modes of operation that can be selected by control words.

Mode 0-Basic I/O (Group A, Group B)
Mode 1-Strobe input/Strobe output (Group A, Group B)
Mode 2-Two-way bus (Port A only)

Operation modes for Group A and Group B can be independently defined by the control word form the MPU. If D_7 is set to "1" in writing a control word into the PPI, operation mode is selected, while of D_7 = "0", the set/reset function for Port C is selected.

5.1.1 Control word to define operation mode

Figure 5.1 shows the control words to define operation mode of the TMP82C55A.

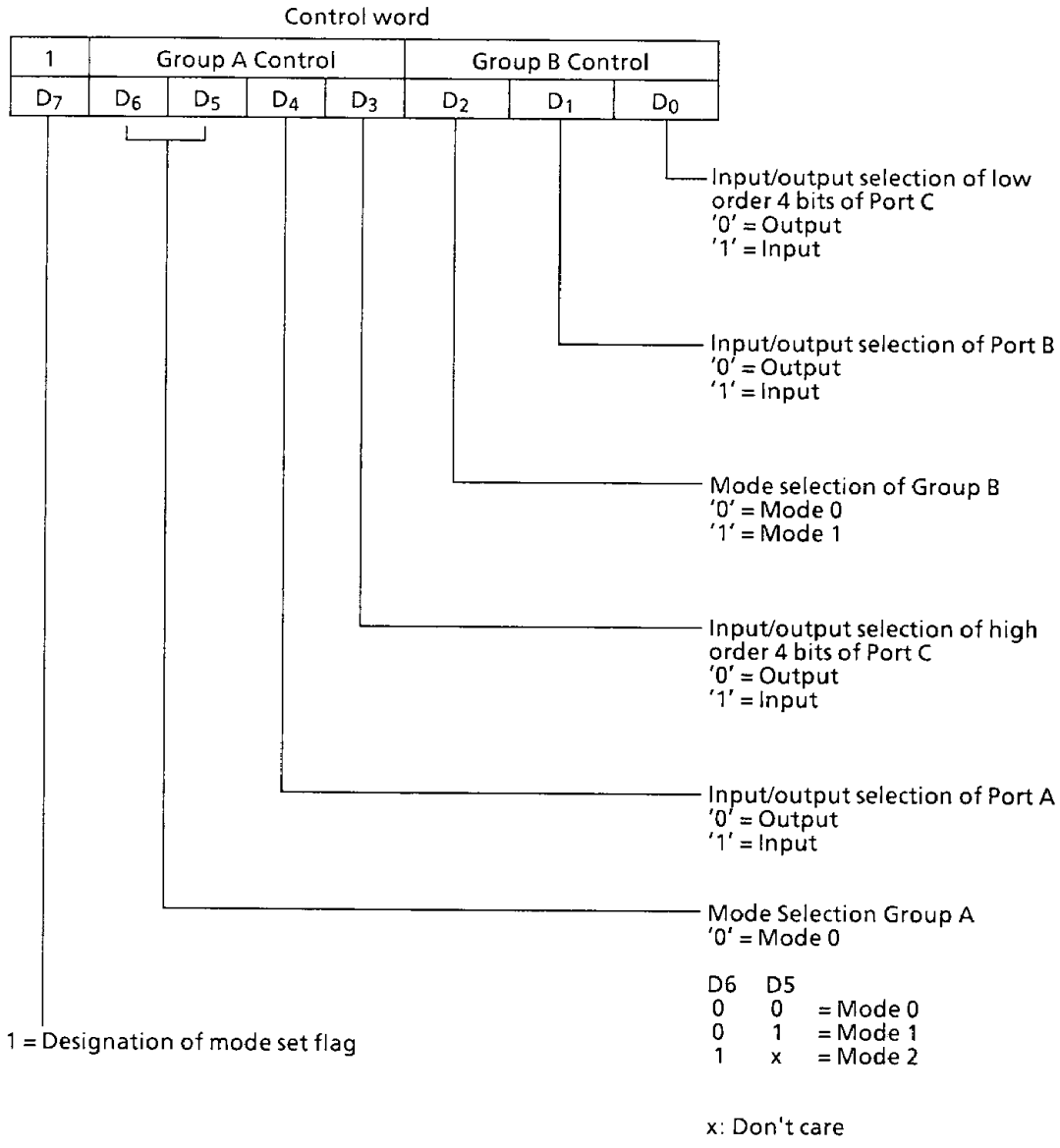


Figure 5.1 Control Word for Mode Selection

5.1.2 Port C bit set/reset control word

Any bit of 8 bits of Port C can be set/reset by Port C bit set/reset control word. Fig. 5.2 shows the Port C bit set/reset control word.

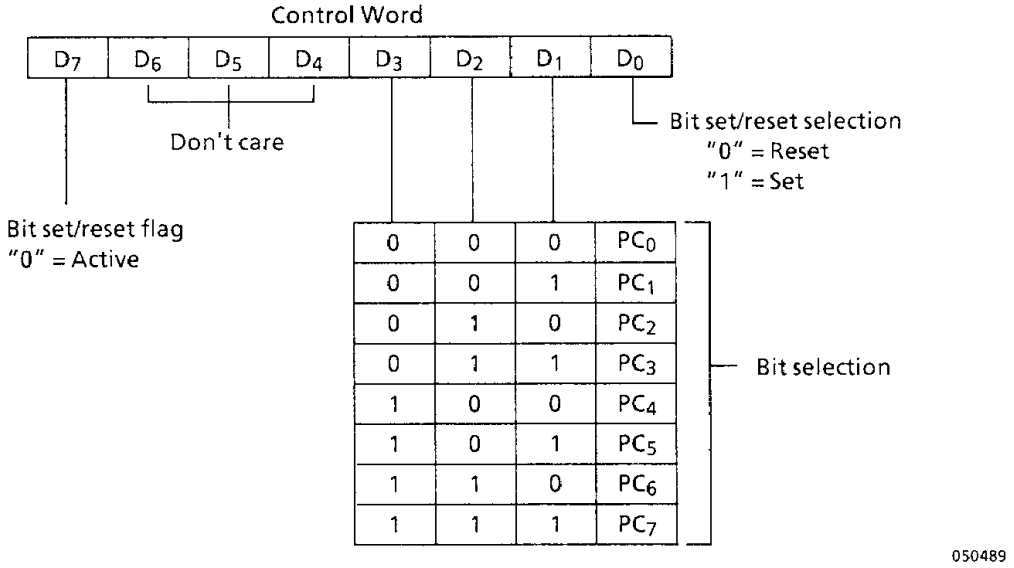


Figure 5.2 Control Word for Bit Set/Reset

5.2 OPERATION MODES

5.2.1 Mode 0 (Basic I/O)

This functional configuration is used for simple input or output operations. No 'handshaking' is required and data is simply written to or read from a specified part. Output data to the ports from MPU are latched out but input data from the ports are not latched.

In Mode 0, 24 I/O terminals are divided into four groups of Port A (8 bits), Port B (8 bits), high order 4 bits of Port C and low order 4 bits of Port C. Each port can be programmed to be input or output. The configuration of each port are determined according to the contents of Bit 4 (D_4), 3 (D_3), 1 (D_1) and 0 (D_0) of the control word for mode selection.

The I/O configuration of each port in Mode 0 are shown in Table 5.2.

Mode Setting Control Word				Port A	Port C (PC_7~PC_4)	Port B	Port C (PC_3~PC_0)
D_4	D_3	D_1	D_0				
0	0	0	0	Out	Out	Out	Out
0	0	0	1	Out	Out	Out	In
0	0	1	0	Out	Out	In	Out
0	0	1	1	Out	Out	In	In
0	1	0	0	Out	In	Out	Out
0	1	0	1	Out	In	Out	In
0	1	1	0	Out	In	In	Out
0	1	1	1	Out	In	In	In
1	0	0	0	In	Out	Out	Out
1	0	0	1	In	Out	Out	In
1	0	1	0	In	Out	In	Out
1	0	1	1	In	Out	In	In
1	1	0	0	In	In	Out	Out
1	1	0	1	In	In	Out	In
1	1	1	0	In	In	In	Out
1	1	1	1	In	In	In	In

050489

Figure 5.3 Port Definition in Mode 0

5.2.2 Mode 1 (Strobe I/O)

In Mode 1, input/output of port data is performed in conjunction with the strobe signals or 'handshaking' signals. Port C is used to control Port A or Port B.

The basic operatings in Mode 1 are as follows:

- Mode 1 can be set for two groups of Group A and Group B.
- Each group consist of 8-bit data port and 4-bit control/data port.
- The 8-bit data port can be set as input or output port.
- The control/data port is used as control or status of the 8-bit data port.

(1) When used as the input port in Mode 1:

- $\overline{STB}$ (Strobe Input)

  At "0", input data is loaded in the internal input latch in the port.

  In this case, a control signal from MPU is not concerned and data is input from the port any time. This data is not read out on the data bus unless MPU executes an input instruction.

- IBF (Input Buffer Full F/F Output)

  When data is loaded in the internal input latch from the port, this output is set to "1". IBF is set ("1") by $\overline{STB}$ input being reset and is reset ("0") by the rising edge of $\overline{RD}$ input.

- INTR (Interrupt Request Output)

  Used for the interrupt process of data loaded in the internal input latch. When $\overline{STB}$ input is at "0" if INTE (INTE flag) in the PPI is in the enabled state ("1"), IBF is set to "1". INTR is set to "1" immediately after the rising edge of this $\overline{STB}$ input and reset to "0" by the falling edge of $\overline{RD}$ input.

  The INTE flag of Group A and Group B are controlled as follows:

  INTEA-Control by bit set/reset of PC_4
  INTEB-Control by bit set/reset of PC_2

(2) When used as the output port in Mode 1:

- $\overline{OBF}$ (Output Buffer Full F/F Output)

  This is a flag which shows that MPU has written data into a specified port. $\overline{OBF}$ is set to becomes "0" at the rising edge of $\overline{WR}$ signal and is set to "1" at the falling edge of $\overline{ACK}$ (Acknowledge input) signal.

- $\overline{ACK}$ (Acknowledge Input)

  $\overline{ACK}$ signal is sent to the PPI as a response from a peripheral device taht received data from the port.

- INTR (Interrupt Request Output)

  When a peripheral device received data from MPU, INTR is set to "1" and the interrupt is requested to MPU. If $\overline{ACK}$ signal is received when INTE flag is in the enable state, $\overline{OBF}$ is set to "1" and INTR signal becomes "1" immediately after the rising edge of $\overline{ACK}$ signal. Further, INTR is reset at the falling edge of $\overline{WR}$ signal when data is written into the PPI by MPU.

  The INTE flags of Group A and Group B are controlled as follows:

  INTEA-Control by bit set/reset of PC_6
  INTEB-Control by bit set/reset of PC_2

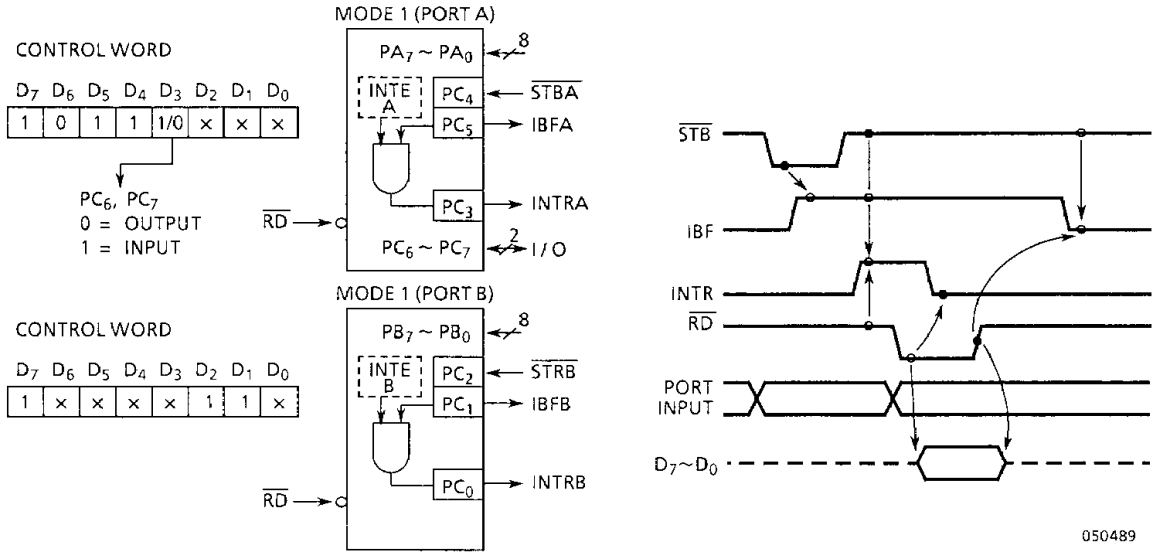
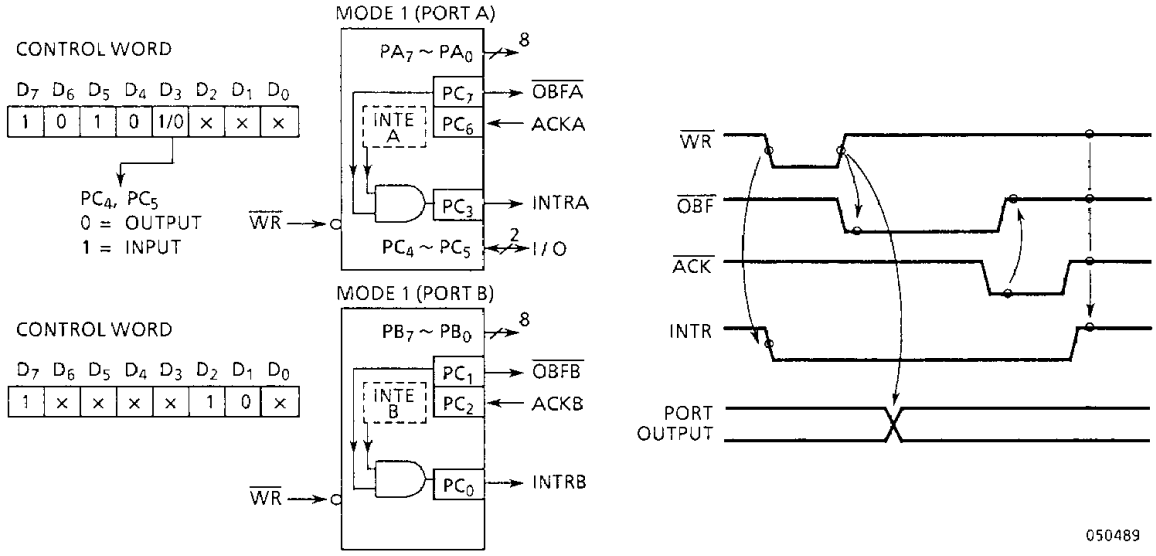


Figure 5.4 Example of Strobe Input in Mode 1



Figuire 5.5 Example of Strobe Output in Mode 1

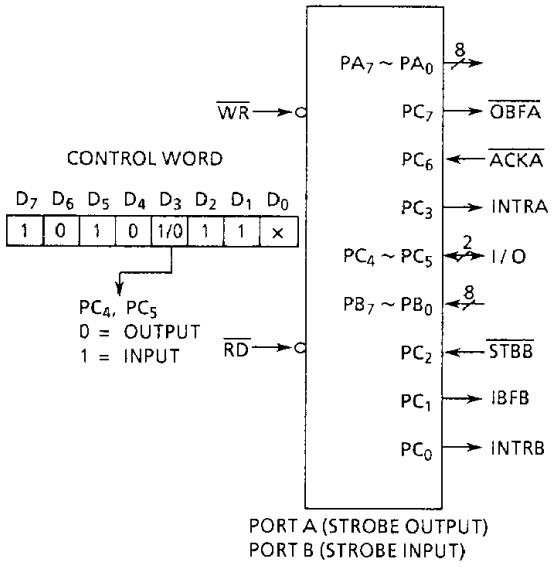
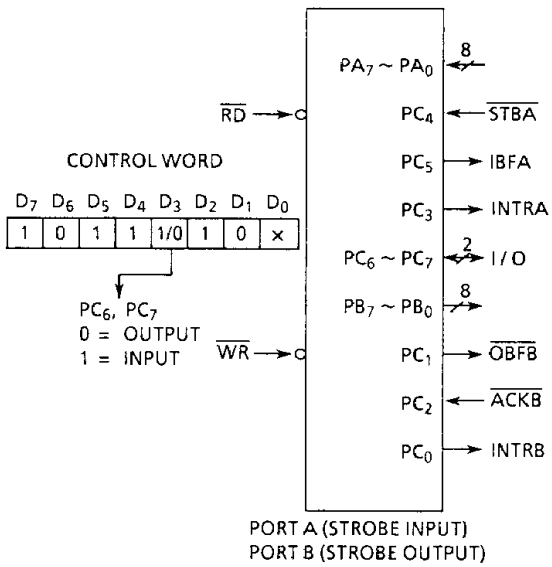


Figure 5.6 Example of Port A Output, Port B Input in Mode 1



050489

Figure 5.7 Example of Port A Input, Port B Output in Mode 1

5.2.3 Mode 2 (Strobed Bidirectional Bus I/O)

In this mode, Port A is used as 8 bits bidirectional bus for data transfer with a peripheral device. This mode is applicable only to Group A, which consists of an 8-bit bidirectional bus (Port A 8-bit) and 5-bit control signals (high order 5 bits of Port C). The bidirectional bus (Port A) has both the internal input and output registers. When group A is set in Mode 2, Group B can be set independently. There are 5 control signals as follows when Group A is used in Mode 2.

- $\overline{OBF}$ (Output buffer Full F/F Output)

  When MPU writes data into of Port A, $\overline{OBF}$ is set to "0" to inform a peripheral device that the PPI is ready to output data. However, Port A is kept in the floating (high impedance) state until $\overline{ACK}$ input signal is received.

- $\overline{ACK}$ (Acknowledge Input)

  When $\overline{ACK}$ signal is set to "0", the data of the 3-state output buffer of Port A is send out. If $\overline{ACK}$ signal is at "1", Port A is in the high impedance state.

- $\overline{STB}$ (Strobe Input)

  When $\overline{STB}$ input is set to "0", the data from peripheral devices are held in the input latch. When the active $\overline{RD}$ signal is input into the PPI, the latched input data are output on the system data bus (D_7-D_0).

- IBF (Input Buffer Full F/F Output)

  When data from peripheral devices are held in the input latch, IBF is set to "1".

- INTR (Interrupt Request Output)

  INTR is the output to request the interrupt to MPU and its function is the same as that in Mode 1. There are two interrupt enable flip-flop (INTE), INTE1 corresponds to INTEA in Mode 1 output and INTE2 to INTEA in Mode 1 input.

  INTE 1-Used to generate INTR signal in conjunction with $\overline{OBF}$ and $\overline{ACK}$ signals, and is controlled by PC_6 bit set/reset.

  INTE 2-Used to generate INTR signal in conjunction with IBF and $\overline{STB}$ signals, and is controlled by PC_4 bit set/reset.

  Fig. 5.8 shows the operating example and the timing diagram in Mode 2.

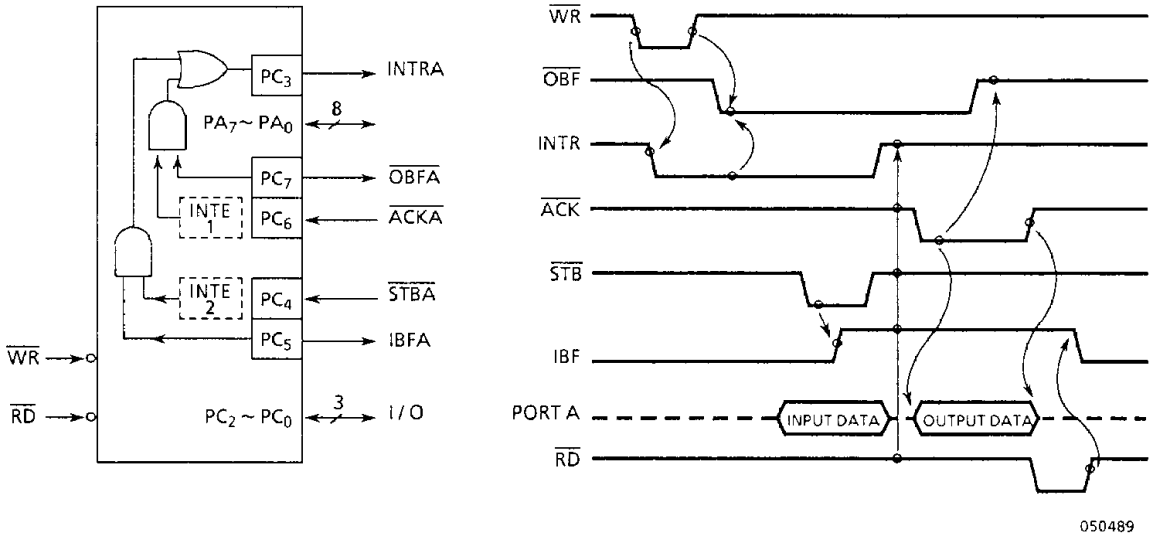


Figure 5.8 Operating Example in Mode 2

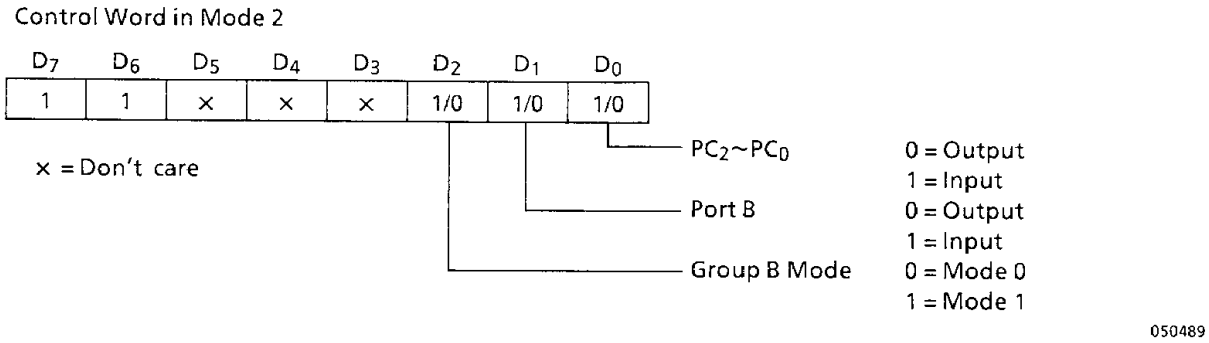


Figure 5.9 Control Word and Configuration in Mode 2

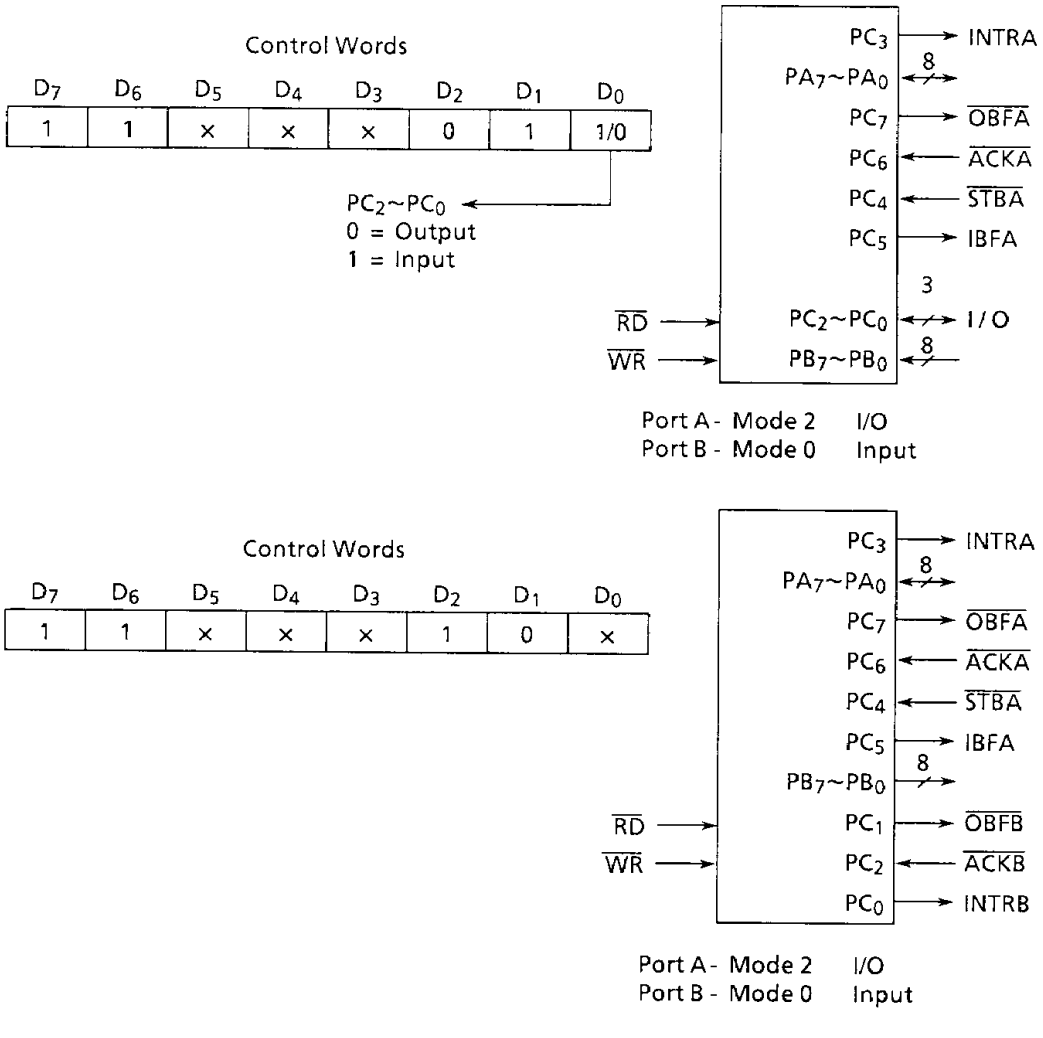


Figure 5.10 Examples in Combination with Mode 2 and Other Mode

5.2.4 Precautions for use in mode 1 and 2

When used in Mode 1 and 2, bits which are not used as control or status in Port C can be used as follow.

If programmed as the input, they are accessed by normal Port C read.

If programmed as the output, high order bits of Port C (PC_7-PC_4) are accessed using the bit set/reset function. As to low order bits of Port C (PC_3-PC_0), in additions to access by the bit set/reset function, only 3 bits can be accessed by normal writing.

5.3 READING PORT C STATUS

When Port C is used as the control port, that is, when Port C is used in Mode 1 or Mode 2, the status information of the control word can be read out by a normal read operation of Port C.

Table 5.2 Status Word Format of Port C

Mode \ Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Mode 1 Input	I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
Mode 1 Output	$\overline{OBFA}$	INTEA	I/O	I/O	INTRA	INTEB	$\overline{OBFB}$	INTRB
Mode 2	$\overline{OBFA}$	INTE1	IBFA	INTE2	INTRA	By Group B Mode		

050489

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{CC}	Supply Voltage	− 0.5 to 7.0	V
V_{IN}	Input Voltage	− 0.5 to V_{CC} + 0.5	V
P_D	Power Dissipation	250	mW
T_{SOLDER}	Soldering Temperature (10 sec)	260	℃
T_{STG}	Storage Temperature	− 65 to + 150	℃
T_{OPR}	Operating Temperature	− 40 to + 85	℃

050489

6.2 DC ELECTRICAL CHARACTERISTICS

TA = − 40℃ to + 85℃, V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		− 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.2	—	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.5mA	—	—	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400μA	2.4	—	—	V
V_{OH2}	Output High Voltage	I_{OH} = -100μA	V_{CC}-0.8	—	—	V
I_{IL}	Input Leak Current	$0 \leqq V_{IN} \leqq V_{CC}$	—	—	± 10	μA
I_{LO}	Output Leak Current (High Impedance State)	$0 \leqq V_{OUT} \leqq V_{CC}$	—	—	± 10	μA
(Note) I_{DAR}	Darlington Drive Current	V_{EXT} = 1.5V R_{EXT} = 1.1kΩ	− 1.0	—	− 5.0	mA
I_{CC1}	Operating Supply Current	I / Ocycle Time 1μsec	—	2.0	5.0	mA
I_{CC2}	Stand-by Supply Current	$\overline{CS} \geqq V_{CC}$-0.2V $V_{IH} \geqq V_{CC}$-0.2V $V_{IL} \leqq$ 0.2V	—	—	10	μA

050489

Note: Applied for optional 8 I/O terminals in Port B and Port C.

6.3 AC ELECTRICAL CHARACTREISTICS

$T_A = -40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

SYMBOL	PARAMETER	AP-2 / AM-2		AP-10 / AM-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{AR}	Address set-up time for $\overline{RD}$ fall	0	—	0	—	ns
t_{RA}	Address hold time for $\overline{RD}$ rise	0	—	0	—	ns
t_{RR}	$\overline{RD}$ pulse width	160	—	150	—	ns
t_{RD}	Delay from $\overline{RD}$ fall to decided data output	—	140	—	100	ns
t_{DF}	Time from $\overline{RD}$ rise to data bus floating	0	40	0	40	ns
t_{RV}	Time from $\overline{RD}$ or $\overline{WR}$ rise to next $\overline{RD}$ or $\overline{WR}$ fall	200	—	150	—	ns
t_{AW}	Address set-up time for $\overline{WR}$ fall	0	—	0	—	ns
t_{WA}	Address holding time for $\overline{WR}$ rise	0	—	0	—	ns
t_{WW}	$\overline{WR}$ pulse width	120	—	120	—	ns
t_{DW}	Bus data set-up time for $\overline{WR}$ rise	100	—	100	—	ns
t_{WD}	Bus data holding time for $\overline{WR}$ rise	0	—	0	—	ns
t_{WB}	Delay from $\overline{WR}$ rise to decided data output	—	350	—	350	ns
t_{IR}	Port data set-up time for $\overline{RD}$ fall	0	—	0	—	ns
t_{HR}	Port data holding time for $\overline{RD}$ rise	0	—	0	—	ns
t_{AK}	$\overline{ACK}$ pulse width	300	—	300	—	ns
t_{ST}	$\overline{STB}$ pulse width	350	—	350	—	ns
t_{PS}	Port data set-up time for $\overline{STB}$ rise	0	—	0	—	ns
t_{PH}	Port data holding time for $\overline{STB}$ rise	150	—	150	—	ns
t_{AD}	Delay from $\overline{ACK}$ fall to decided data output	—	300	—	300	ns
t_{KD}	Time from $\overline{ACK}$ rise up to port (Port A in Mode 2) floating	25	250	20	250	ns
t_{WOB}	Delay from $\overline{WR}$ rise to $\overline{OBF}$ fall	—	300	—	300	ns
t_{AOB}	Delay from $\overline{ACK}$ fall to $\overline{OBF}$ rise	—	350	—	350	ns
t_{SIB}	Delay from $\overline{STB}$ fall to IBF rise	—	300	—	300	ns
t_{RIB}	Delay from $\overline{RD}$ fall to $\overline{IBF}$ rise	—	300	—	300	ns
t_{RIT}	Delay from $\overline{RD}$ fall to INTR fall	—	400	—	400	ns
t_{SIT}	Delay from $\overline{ACK}$ rise to INTR rise	—	300	—	300	ns
t_{AIT}	Delay from $\overline{ACK}$ rise to INTR rise	—	350	—	350	ns
t_{WIT}	Delay from $\overline{WR}$ rise to INTR	—	450	—	450	ns

050489

Note : 1. When the power supply is turned ON, reset pulse duration must be active for at least 500 ns or more.

2. AC Measuring Point Input Voltage $V_{IH} = 2.4V$, $V_{IL} = 0.45V$
Output Voltage $V_{OH} = 2.2V$, $V_{OL} = 0.8V$
$CL = 150pF$.

6.4 CAPACITANCE

$T_A = 25℃$, $V_{CC} = V_{SS} = 0V$

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	f_C = 1MHz (*)	—	—	10	pF
C_{OUT}	Output Capacitance		—	—	20	pF

050489

(*) : All terminals except that to be measured should be earthed.

7. TIMING DIAGRAM

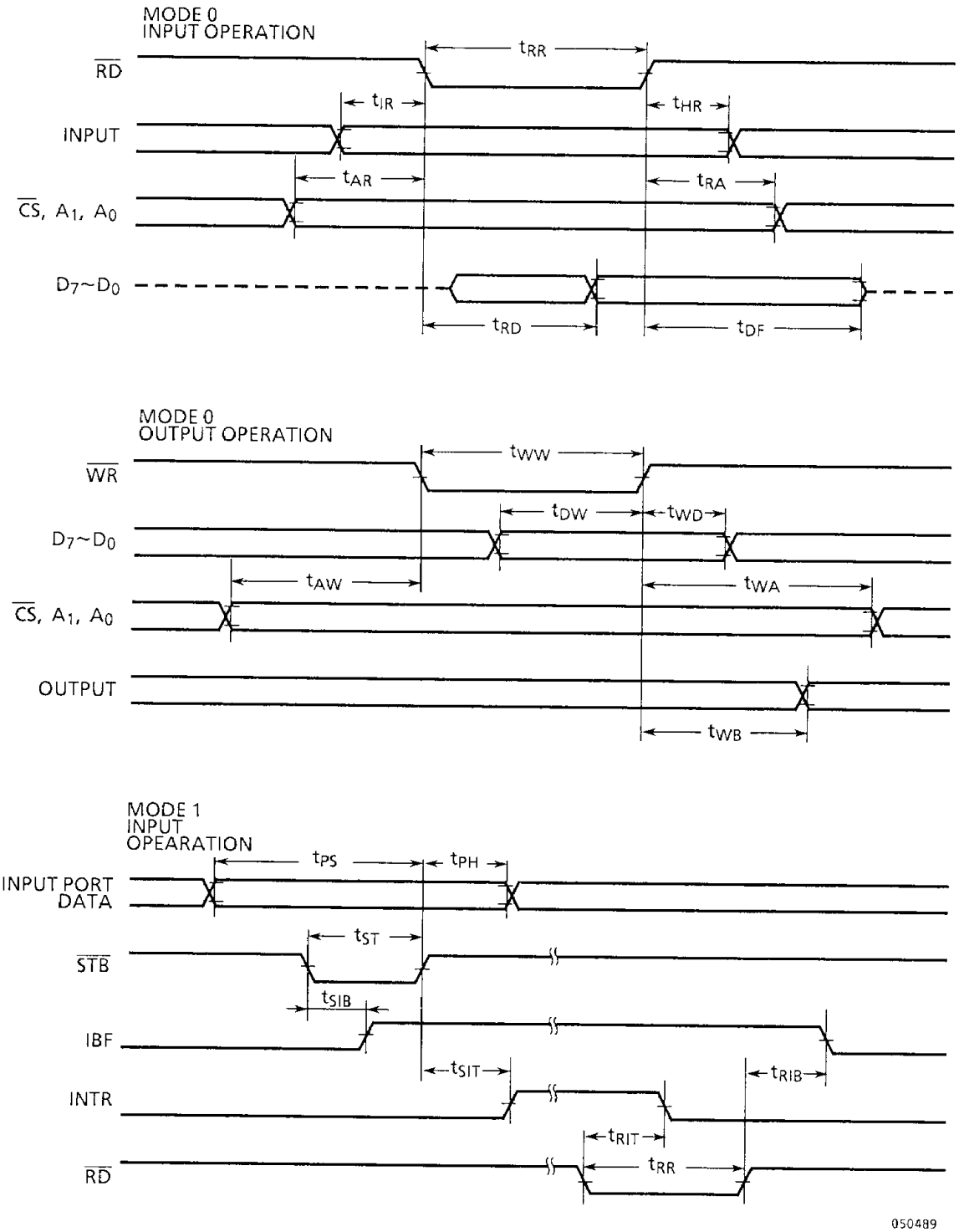


Figure 7.1 Timing Diagram

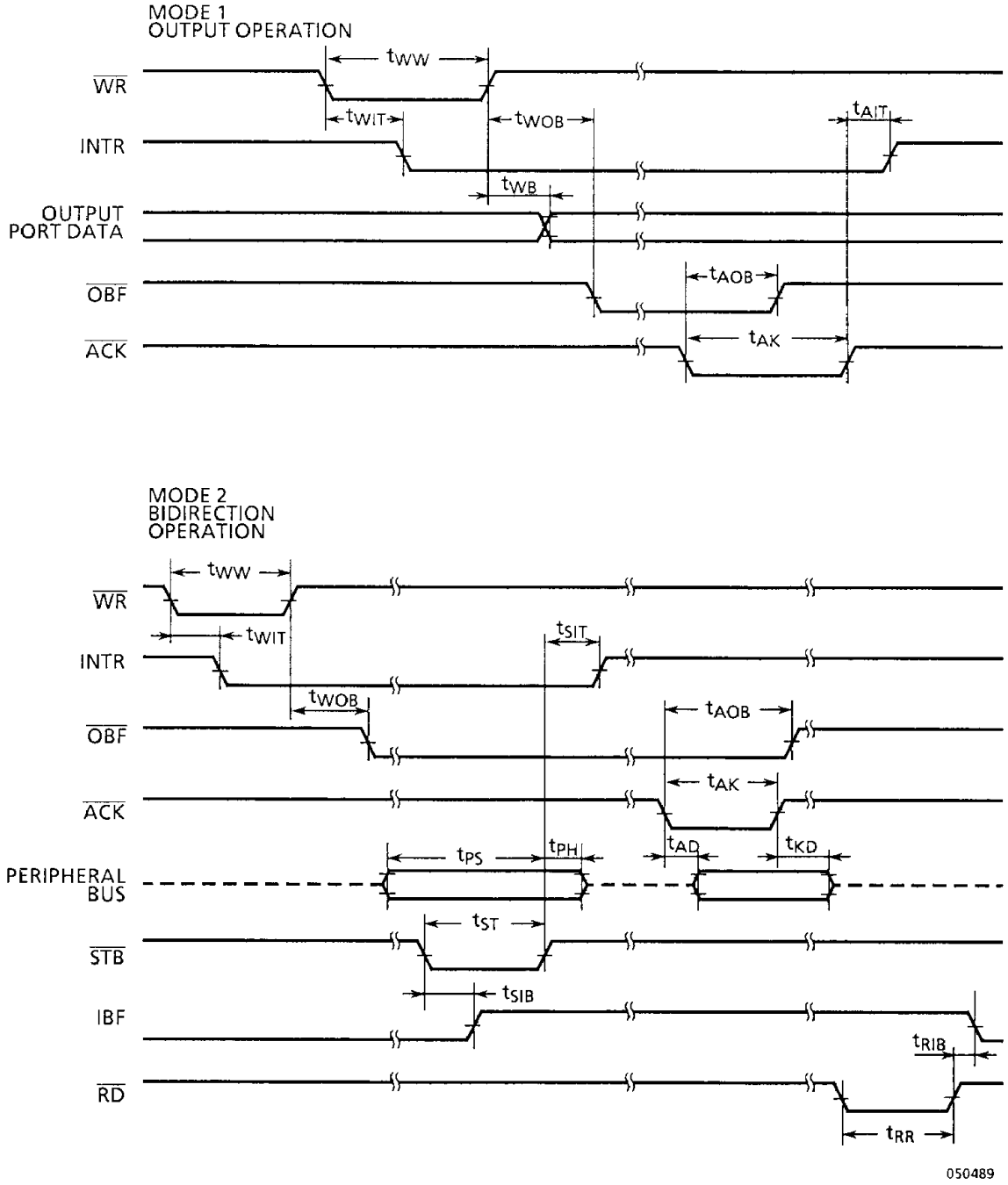


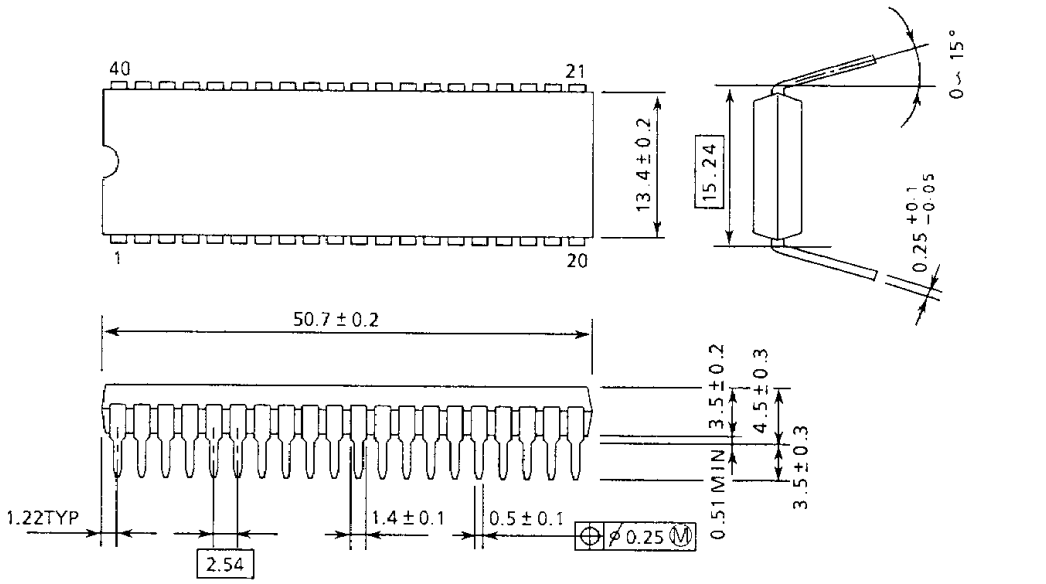
Figure 7.2 Timing Diagram

8. PACKAGE DIMENSION

8.1 PLASTIC PACKGE

DIP40-P-600

Unit : mm



270289

Note : Each lead pitch is 2.54mm, and all the leads are located witchin ±0.25mm from their theoretical positions with respect to No.1 and No.4 leads.