100 V, 18 A, 34.7 mΩ Low $R_{DS(ON)}$
N ch Trench Power MOSFET

FKI10531

Features

- $V_{(BR)DSS}$ ---------- 100 V (I_D = 100 µA)
- I_D ---------- 18 A
- $R_{DS(ON)}$ -------- 54.5 mΩ max. (V_{GS} = 10 V, I_D = 11.9 A)
- Q_g ------- 9.0 nC (V_{GS} = 4.5 V, V_{DS} = 50 V, I_D = 11.9 A)

- Low Total Gate Charge
- High Speed Switching
- Low On-Resistance
- Capable of 4.5 V Gate Drive
- 100 % UIL Tested
- RoHS Compliant

Package

TO-220F

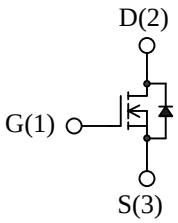
(1) G (2) D (3) S

Not to scale

Applications

- DC-DC converters
- Synchronous Rectification
- Power Supplies

Equivalent circuit



Absolute Maximum Ratings

- Unless otherwise specified, T_A = 25 °C

Parameter	Symbol	Test conditions	Rating	Unit
Drain to Source Voltage	V_{DS}		100	V
Gate to Source Voltage	V_{GS}		± 20	V
Continuous Drain Current	I_D	T_C = 25 °C	18	A
Pulsed Drain Current	I_{DM}	PW ≤ 100µs Duty cycle ≤ 1 %	35	A
Continuous Source Current (Body Diode)	I_S		18	A
Pulsed Source Current (Body Diode)	I_{SM}	PW ≤ 100µs Duty cycle ≤ 1 %	35	A
Single Pulse Avalanche Energy	E_{AS}	V_{DD} = 50 V, L = 1 mH, I_{AS} = 6.8 A, unclamped, R_G = 4.7 Ω Refer to Figure 1	47	mJ
Avalanche Current	I_{AS}		13.3	A
Power Dissipation	P_D	T_C = 25 °C	32	W
Operating Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{STG}		− 55 to 150	°C

Thermal Characteristics

• Unless otherwise specified, T_A = 25 °C

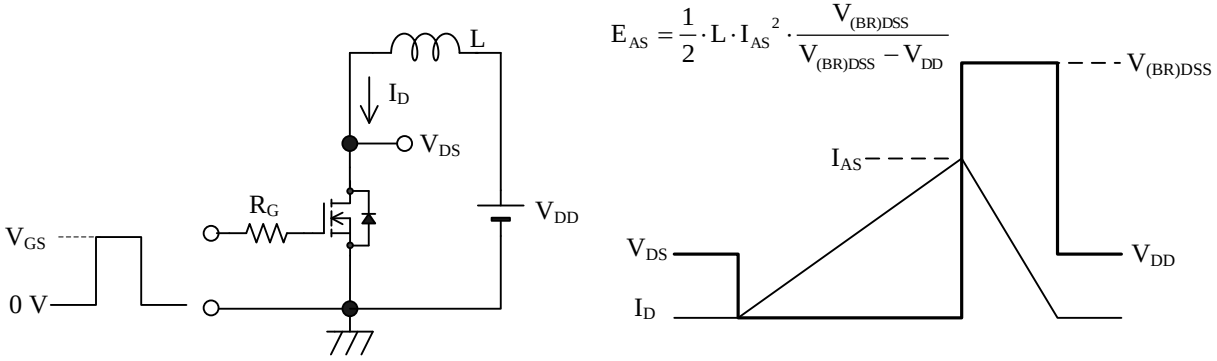
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance (Junction to Case)	$R_{\theta JC}$		−	−	3.9	°C/W
Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$		−	−	62.5	°C/W

Electrical Characteristics

• Unless otherwise specified, T_A = 25 °C

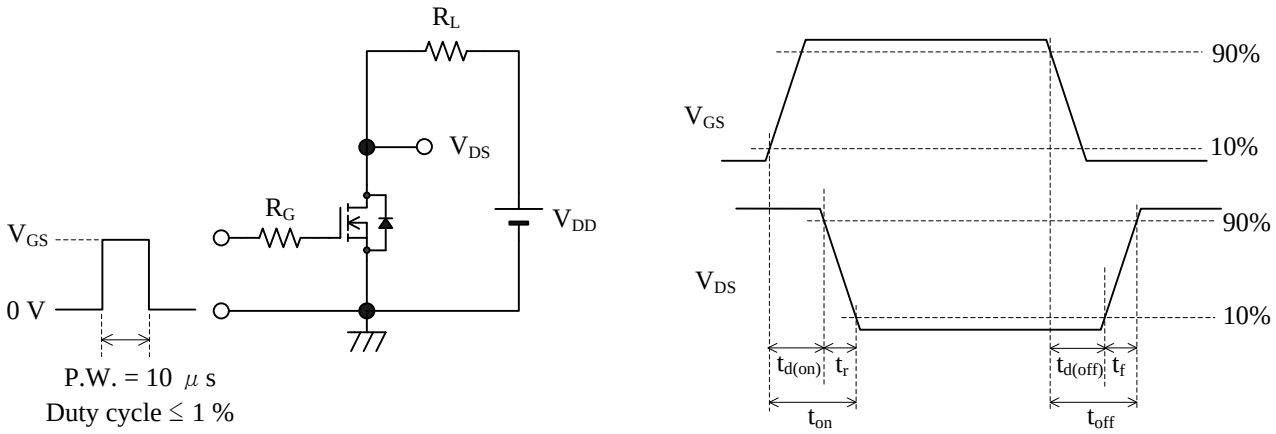
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	100	−	−	V
Drain to Source Leakage Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	−	−	100	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V	−	−	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 350 µA	1.0	2.0	2.5	V
Static Drain to Source On-Resistance	$R_{DS(ON)}$	I_D = 11.9 A, V_{GS} = 10 V	−	34.7	54.5	mΩ
		I_D = 6.0 A, V_{GS} = 4.5 V	−	36.5	56.5	mΩ
Gate Resistance	R_G	f = 1 MHz	−	2.3	−	Ω
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz	−	1530	−	pF
Output Capacitance	C_{oss}		−	125	−	
Reverse Transfer Capacitance	C_{rss}		−	51	−	
Total Gate Charge (V_{GS} = 10 V)	Q_{g1}	V_{DS} = 50 V I_D = 11.9 A	−	19.9	−	nC
Total Gate Charge (V_{GS} = 4.5 V)	Q_{g2}		−	9.0	−	
Gate to Source Charge	Q_{gs}		−	3.6	−	
Gate to Drain Charge	Q_{gd}		−	2.6	−	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V I_D = 11.9 A V_{GS} = 10 V, R_G = 4.7 Ω Refer to Figure 2	−	3.0	−	ns
Rise Time	t_r		−	2.8	−	
Turn-Off Delay Time	$t_{d(off)}$		−	13.7	−	
Fall Time	t_f		−	6.0	−	
Source to Drain Diode Forward Voltage	V_{SD}	I_S = 11.9 A, V_{GS} = 0 V	−	0.9	1.5	V
Source to Drain Diode Reverse Recovery Time	t_{rr}	I_F = 11.9 A di/dt = 100 A/µs Refer to Figure 3	−	40.7	−	ns
Source to Drain Diode Reverse Recovery Charge	Q_{rr}		−	68.2	−	nC

Test Circuits and Waveforms



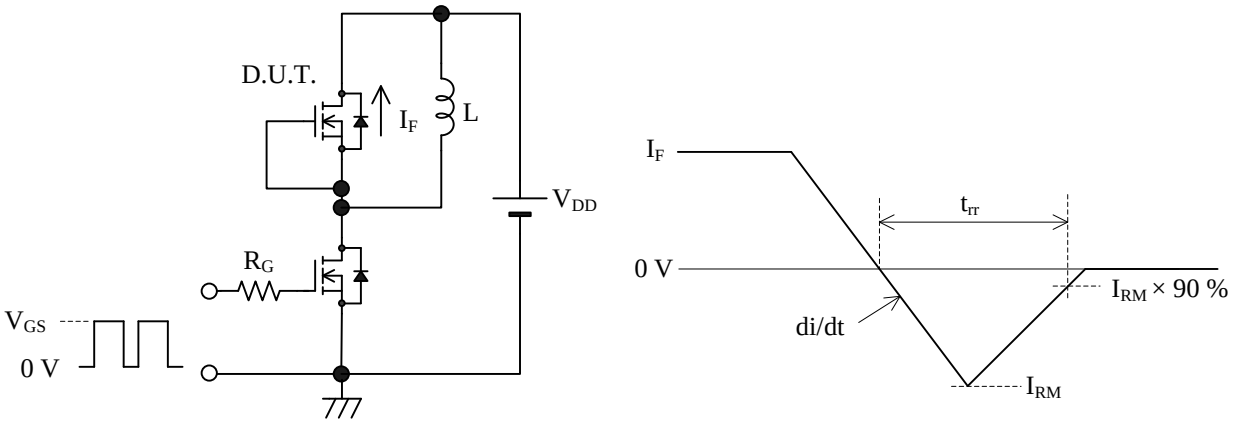
(a) Test Circuit (b) Waveform

Figure 1 Unclamped Inductive Switching



(a) Test Circuit (b) Waveform

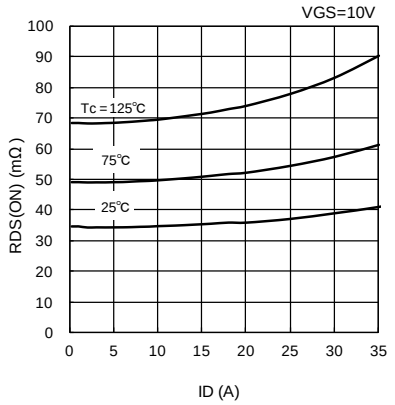
Figure 2 Switching Time



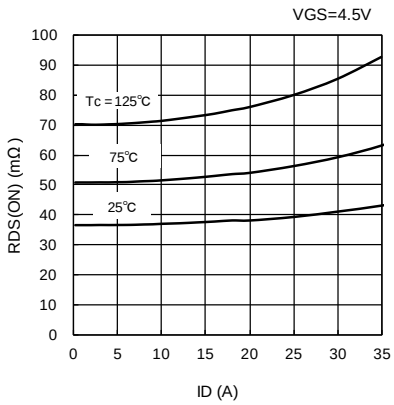
(a) Test Circuit (b) Waveform

Figure 3 Diode Reverse Recovery Time

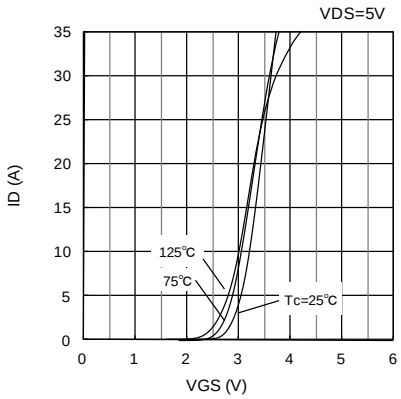
RDS(ON)-ID characteristics (typical)



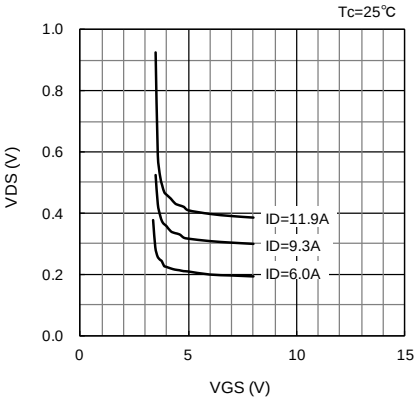
RDS(ON)-ID characteristics (typical)



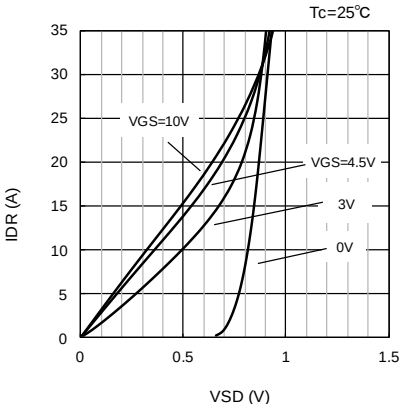
ID-VGS characteristics (typical)



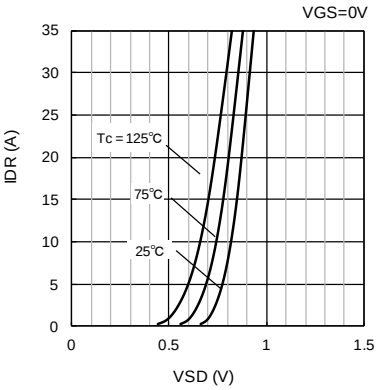
VDS-VGS characteristics (typical)



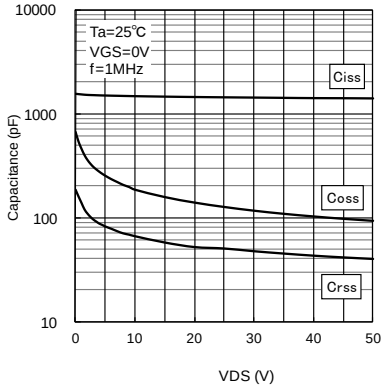
IDR-VSD characteristics (typical)



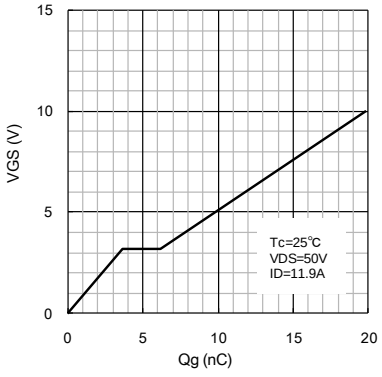
IDR-VSD characteristics (typical)



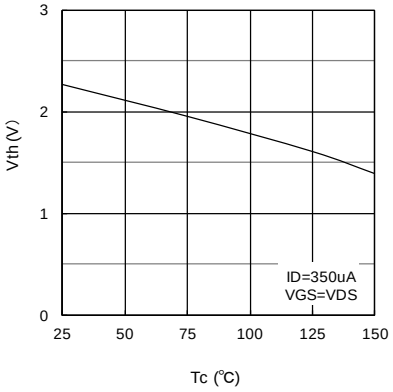
Capacitance-VDS characteristics (typical)



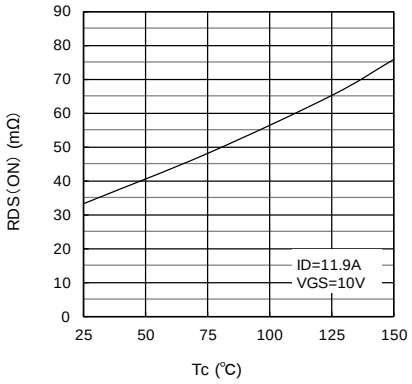
VGS - Qg characteristics (typical)



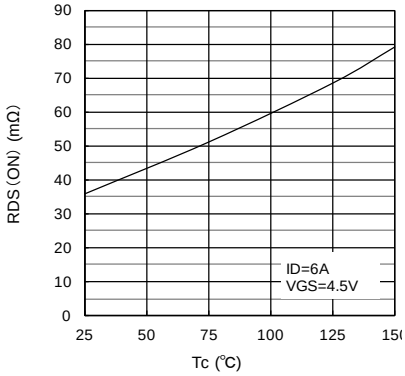
Vth-Tc characteristics (typical)



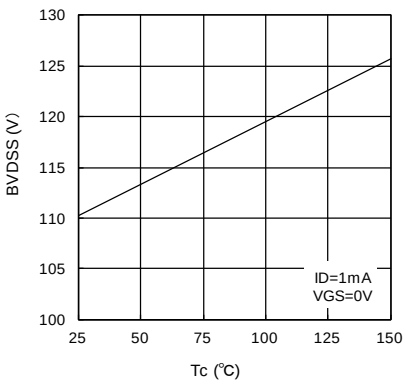
RDS(ON)-Tc characteristics (typical)



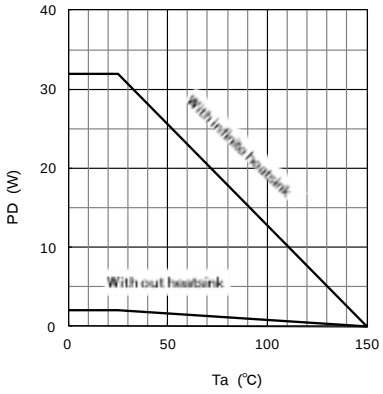
RDS(ON)-Tc characteristics (typical)



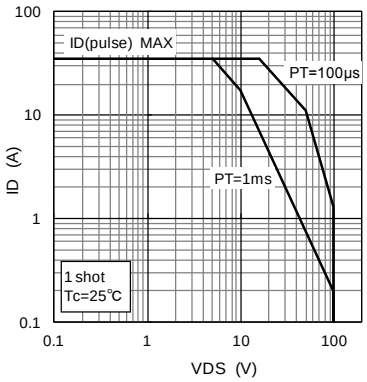
BVDSS-Tc characteristics (typical)



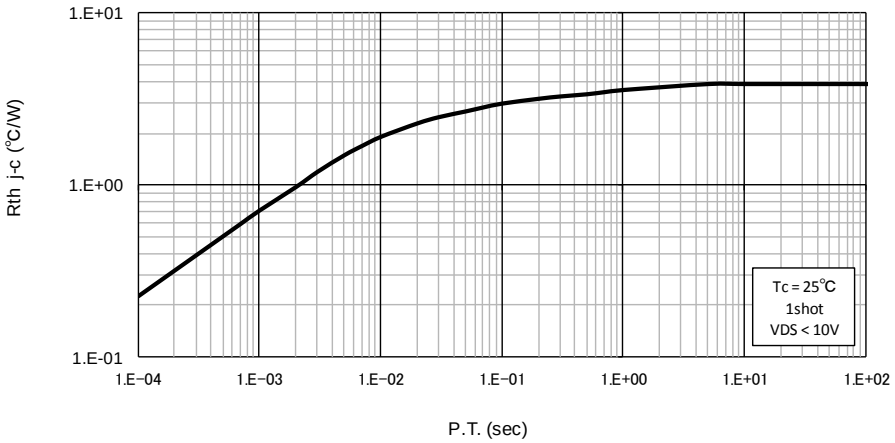
PD-Ta Derating



SAFE OPERATING AREA

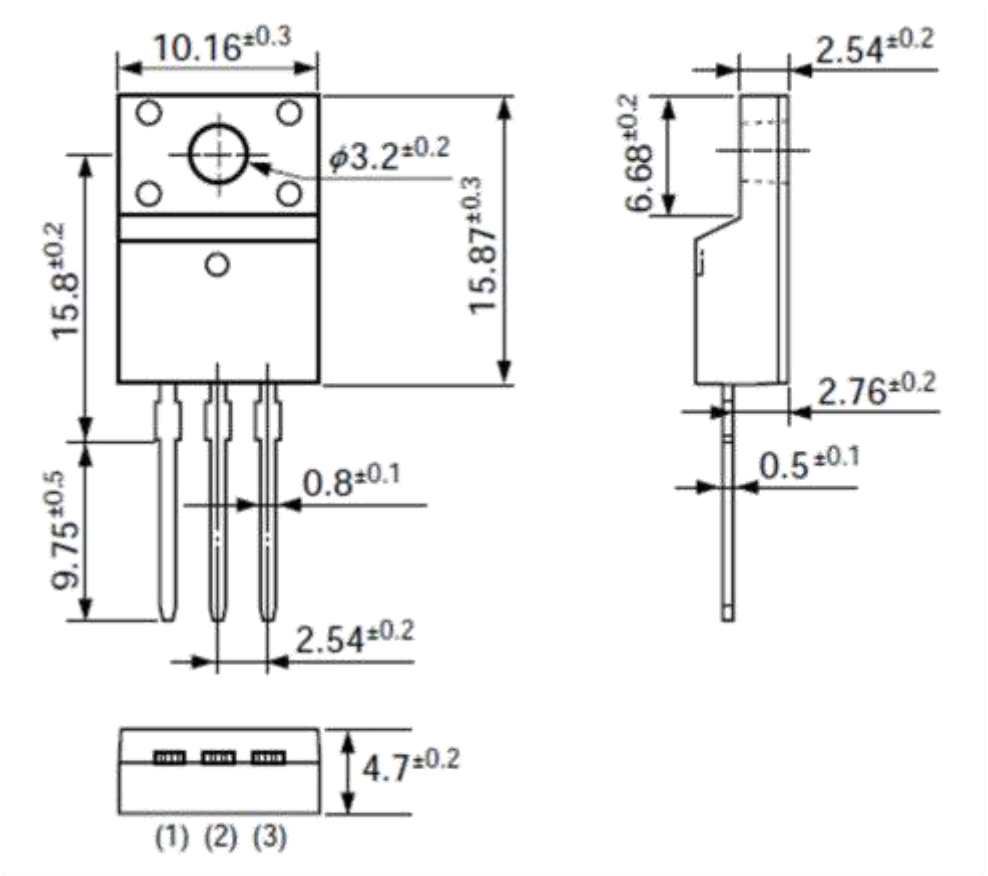


TRANSIENT THERMAL RESISTANCE - PULSE WIDTH



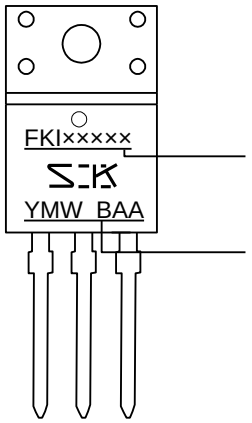
Package Outline

TO-220F



NOTES:
1) Dimension is in millimeters
2) Pb-free. Device composition compliant with the RoHS directive

Marking Diagram



Part Number

Lot Number

Y is the Last digit of the year (0 to 9)

M is the Month (1 to 9, O, N or D)

W is the Week (1st to 5th week of every month)

B expresses Pb free pins

A is the suffix No.