October 1992
Edition 2.0

FUJITSU

DATA SHEET

MBM27C64-20/-25/-30

CMOS 64K-BIT UV EPROM

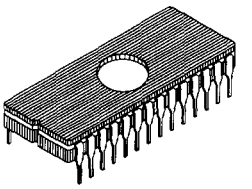
CMOS 65,536-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM27C64 is a high speed 65,536-bit static complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

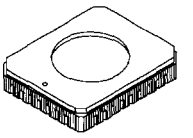
A 28-pin dual-in-line package with a transparent lid and 32-pad Leadless-Chip-Carrier (LCC) are used to package the MBM27C64. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C64 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8,192 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.
This specification is applied to "RA"-version.

- CMOS power consumption: 550µW max. Standby
  165mW max. Active
- 8,192 words by 8 bits organization, fully decoded
- Simple programming requirements
- Single location programming
- Programs with one 50ms or 1ms pulse
- No clock required (fully static operation)
- TTL compatible inputs and outputs
- Three state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Fast access time:
  200ns max.(MBM27C64-20)
  250ns max.(MBM27C64-25)
  300ns max.(MBM27C64-30)
- Single +5V operation
- Standard 28-pin ceramic DIP: (Suffix: Z)
- Standard 32-pad ceramic LCC: (Suffix: CV)
- This specification is applied to "RA"-version.

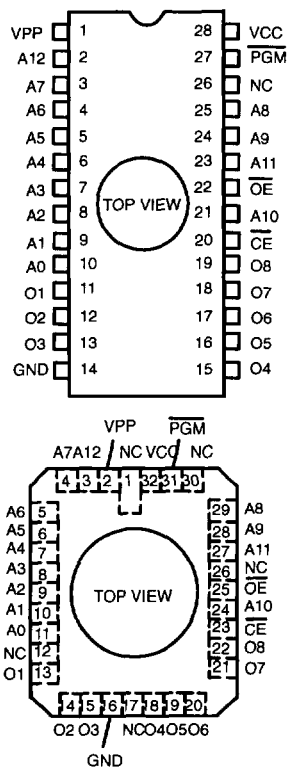


CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-A01

PIN ASSIGNMENT



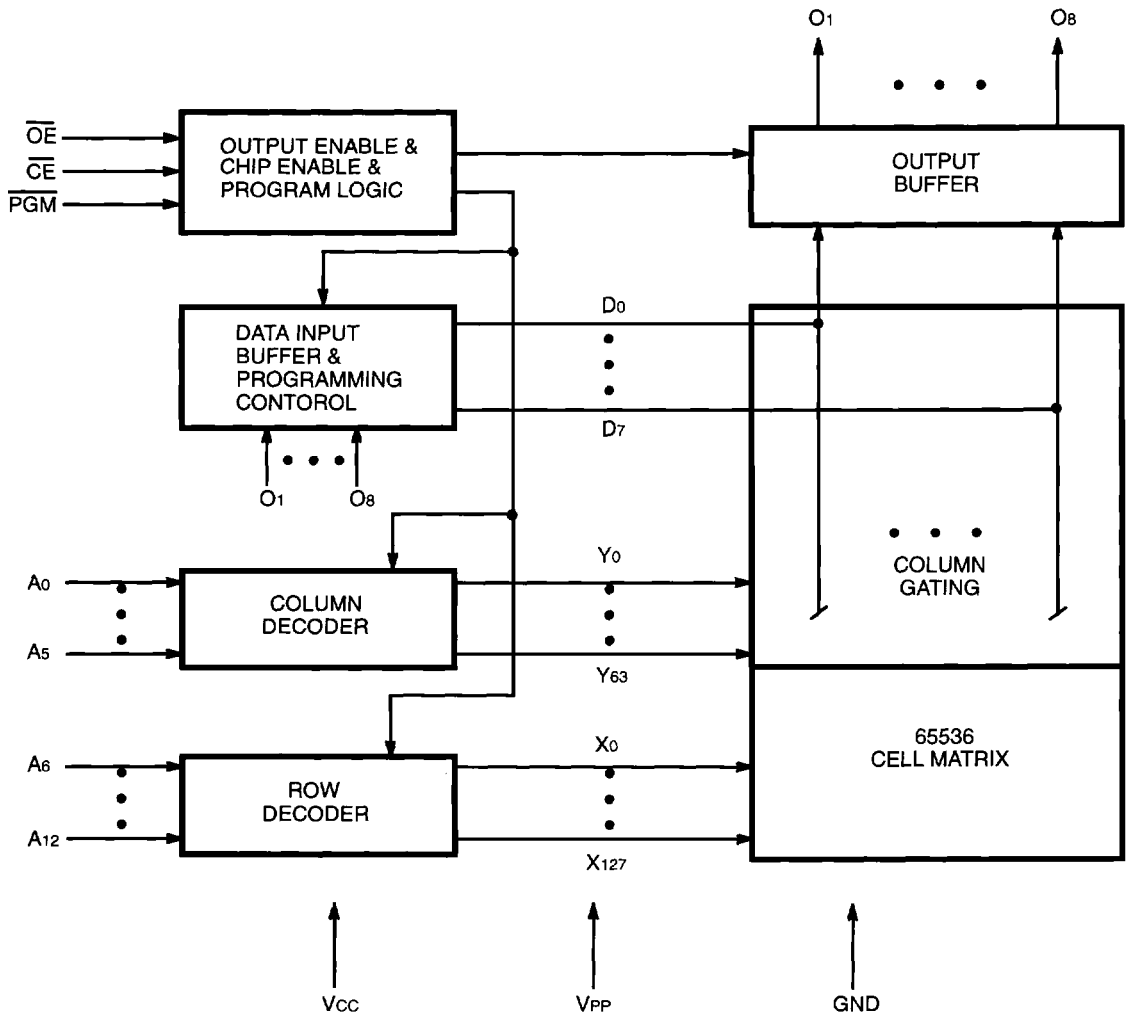
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{STG}	−65 to +125	°C
Inputs/Outputs with Respect to GND	V_{IN}, V_{OUT}	−0.6 to V_{CC}+0.3	V
V_{PP} with Respect to GND	V_{PP}	−0.6 to +22	V
V_{CC} with Respect to GND	V_{CC}	−0.6 to +7	V

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MBM27C64 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	–	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	–	8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Function / Mode	Address Input	Data I/O	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Vcc	VPP	GND
Read	AIN	DOUT	VIL	VIL	VIH	Vcc	Vcc	GND
Output Disable	AIN	High–Z	VIL	VIH	Don't Care	Vcc	Vcc	GND
				Don't Care	VIL			
Standby	Don't Care	High–Z	VIH	Don't Care	Don't Care	Vcc	Vcc	GND
Program	AIN	DIN	VIL	VIH	VIL	VPP	VPP	GND
Program Verify	AIN	DOUT	VIL	VIL	VIH	Vcc	VPP	GND
Program Inhibit	Don't Care	High–Z	VIH	Don't Care	Don't Care	Vcc	VPP	GND

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Vcc Supply Voltage*	Vcc	4.5	5.0	5.5	V	0°C to +70°C
VPP Supply Voltage	VPP	Vcc–0.6	–	Vcc+0.6	V	
Input High Voltage	VIH	2.0	–	Vcc+0.3	V	
Input Low Voltage	VIL	–0.1	–	0.8	V	

Note: *Vcc must be applied either before or coincident with VPP and removed either after or coincident with VPP.

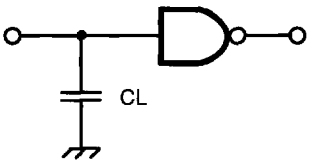
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (VIN = 5.5V)	$\lvert I_{LI} \rvert$			10	µA
Output Leakage Current (VOUT = 5.5V)	$\lvert I_{LO} \rvert$			10	µA
VPP Supply Current	IPP		1	100	µA
VPP Standby Current ($\overline{CE}$ = VIH)	ISB1			1	mA
Vcc Standby Current ($\overline{CE}$ = Vcc –0.3V to Vcc + 0.3V, IOUT = 0mA)	ISB2		1	100	µA
Vcc Active Current ($\overline{CE}$ = VIL)	ICC1			30	mA
Vcc Operation Current (f = 4MHz, IOUT = 0mA)	ICC2			30	mA
Output Low Voltage (IOL = 2.1mA)	VOL			0.45	V
Output High Voltage (IOH = –400µA)	VOH	2.4			V

Fig. 2 – AC TEST CONDITIONS (INCLUDING PROGAMMING)

Input Pulse Levels:	0.8V to 2.2V
Input Rise/Fall Time:	≤20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and CL = 100pF



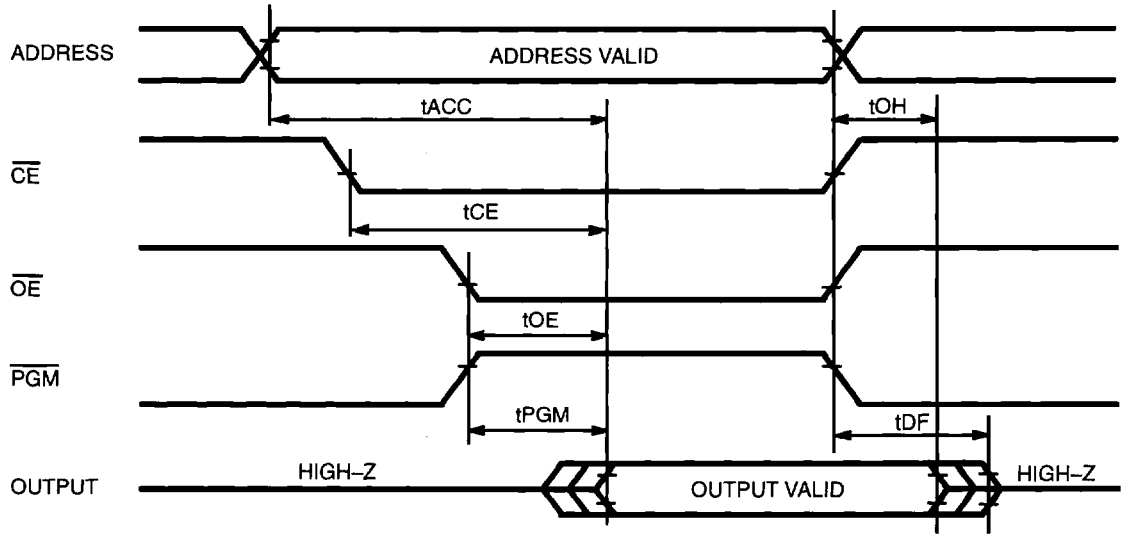
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C64-20			MBM27C64-25			MBM27C64-30			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address to Output Delay ($\overline{CE}$ = $\overline{OE}$ = VIL, $\overline{PGM}$ = VIH)	tACC			200			250			300	ns
$\overline{CE}$ to Output Delay ($\overline{OE}$ = VIL, $\overline{PGM}$ = VIH)	tCE			200			250			300	ns
$\overline{OE}$ to Output Delay ($\overline{CE}$ = VIL,)	tOE			70			100			120	ns
$\overline{PGM}$ to Output Delay ($\overline{CE}$ = $\overline{OE}$ = VIL)	tPGM			70			100			120	ns
Output Enable High to Output Float (See Note)	tDF	0		60	0		60	0		60	ns
Address to Output Hold	tOH	0			0			0			ns

Notes: tDF is specified from $\overline{CE}$, $\overline{OE}$, or $\overline{PGM}$, whichever occurs first.

OPERATION TIMING DIAGRAM



Notes: (1) $\overline{OE}$ may be delayed up to tACC–tOE after the falling edge of $\overline{CE}$ without impact on tACC.
(2) tDF is specified from $\overline{CE}$, $\overline{OE}$, or $\overline{PGM}$, whichever occurs first.

PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM27C64 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig.15). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 16). In the initial state, the cell has a low threshold (VTH1) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (VTH0), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (VTHS), as indicated by the dotted line in Fig. 16.

Fig. 15 – MEMORY CELL

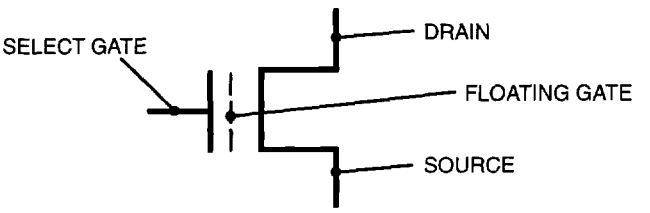
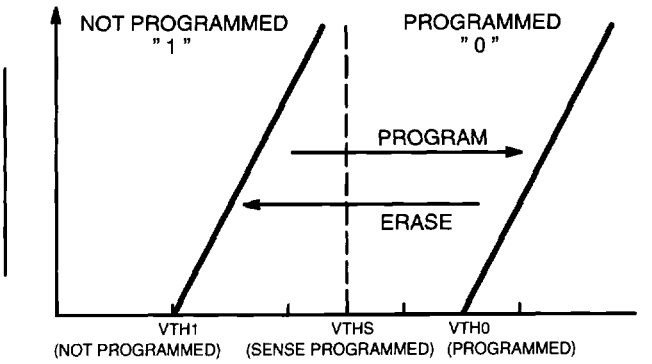


Fig. 16 – MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C64 has all 65,536 bits in the "1", or high, state. "0's" are loaded into the MBM27C64 through the procedure of programming.

Normal Programming

The programming mode is entered when +21V is applied to the VPP pin and CE and PGM are both at VIL. During programming, CE is kept at VIL. A 0.1µF capacitor between VPP and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL Low-level pulse is applied to the PGM input to accomplish the programming. The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the PGM input is prohibited when programming.

Quick Programming

The programming mode is entered when +21V and +6V are applied to the VPP pin and VCC pin respectively, and CE, PGM and OE are VIL and VIH respectively. During Programming, CE is kept at VIL. A 0.1µF capacitor between VPP and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit pattern are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 msec, TTL low-level pulse is applied to the PGM pin and after that additional pulse is applied to the PGM pin to accomplish the programming.

Procedure of quick programming (Refer to the attached flow chart.)

1) Input the start address (Address = G)
2) Set the VCC = 6V and VPP = 21V
3) Data input
4) Compare the input data. If data are FF, jump to the 11). If data are not FF, proceed the next step.
5) Set the number of programming pulse to 0. (X = 0)
6) Apply ONE programming pulse to PGM pin (tPW = 1 ms Typ.).

7) Count the programming pulse (X = X + 1)
8) Compare the number of programming pulse. If X = 20, jump to the 10). If X< 20, proceed the next step.
9) Verify the data. If programmed data are same as input data, proceed the next step. If programming data are not same as input data, repeat the 6) through 8).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1 ms x X or X ms x 1).
11) Compare the address. If the programmed address is not end address, is end address, proceed the next step.
12) Verify the data. If programmed data are not same as input data, the part is no good. If programmed data are same as input data, programming is end.

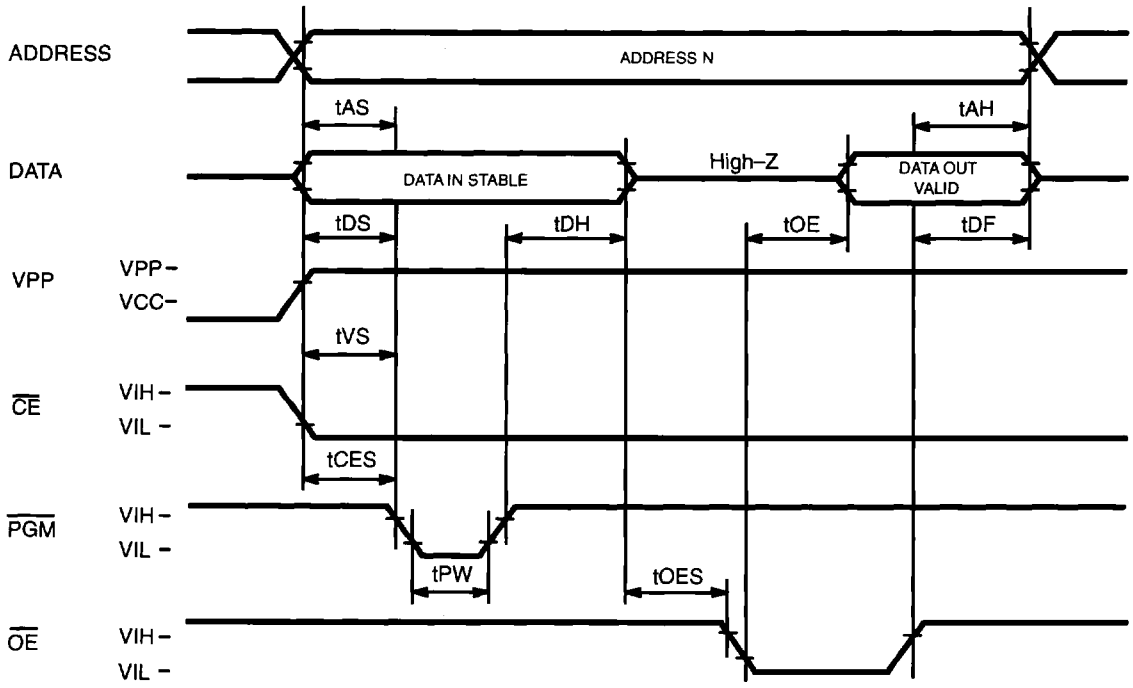
All that is required is that one 1 msec program pulse be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 1.05 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C64 to an ultra-violet light source. A dosage of 15W–seconds/cm is required to completely erase an MBM27C64. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm² for 15 to 20 minutes. The MBM27C64 should be about one all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C64 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM27C64, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASING INFORMATION (Continued)

1. Normal Programming

DC CHARACTERISTICS

(TA = 25±5°C, VCC = 5V±5%, VPP = 21 ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (VIN = 5.25V/0.45V)	$\|I_{LI}\|$			10	µA
VPP Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = VIL)	IPP			40	mA
VCC Supply Current	ICC			30	mA
Input Low Level	VIL	–0.1		0.8	V
Input High Level	VIH	2.0		VCC +0.3	V
Output Low Voltage During Verify (IOL = 2.1 mA)	VOL			0.45	V
Output High Voltage During Verify (IOH = –400µA)	VOH	2.4			V

Note: (1) VCC must be applied either coincidently or before VPP and removed either coincidently or after VPP.
(2) VPP must not be 22 volts or more including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining VPP = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = VIL, VPP must not be switched from 5 volts to 21 volts or vise-versa.

AC CHARACTERISTICS

(TA = 25±5°C, VCC = 5V±5%, VPP = 21 ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup TIme	t_{DS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{DH}	2			µs
Chip Enable to Output Float Delay	t_{DF}	0		130	µs
Data Valid from Output Enable	t_{OE}			150	µs
VPP Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	25	50	55	µs

2. Quick Programming

DC CHARACTERISTICS

(TA = 25±5°C, VCC = 6V±0.25V, VPP = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (VIN = 6.25V/0.45V)	$\|I_{LI}\|$			10	µA
VPP Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = VIL)	IPP			40	mA
VCC Supply Current	ICC			30	mA
Input Low Level	VIL	–0.1		0.8	V
Input High Level	VIH	2.0		VCC +0.3	V
Output Low Voltage During Verify (IOL = 2.1 mA)	VOL			0.45	V
Output High Voltage During Verify (IOH = –400µA)	VOH	2.4			V

Note: (1) VCC must be applied either coincidently or before VPP and removed either coincidently or after VPP.
(2) VPP must not be 22 volts or more including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining VPP = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = VIL, VPP must not be switched from VCC to VPP volts or vise-versa.

AC CHARACTERISTICS

(TA = 25±5°C, VCC = 6V±0.25V, VPP = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup TIme	t_{DS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{DH}	2			µs
Chip Enable to Output Float Delay	t_{DF}	0		130	µs
Data Valid from Output Enable	t_{OE}			150	µs
VPP Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.95	1	1.05	µs

PROGRAMMING/ERASING INFORMATION (Continued)

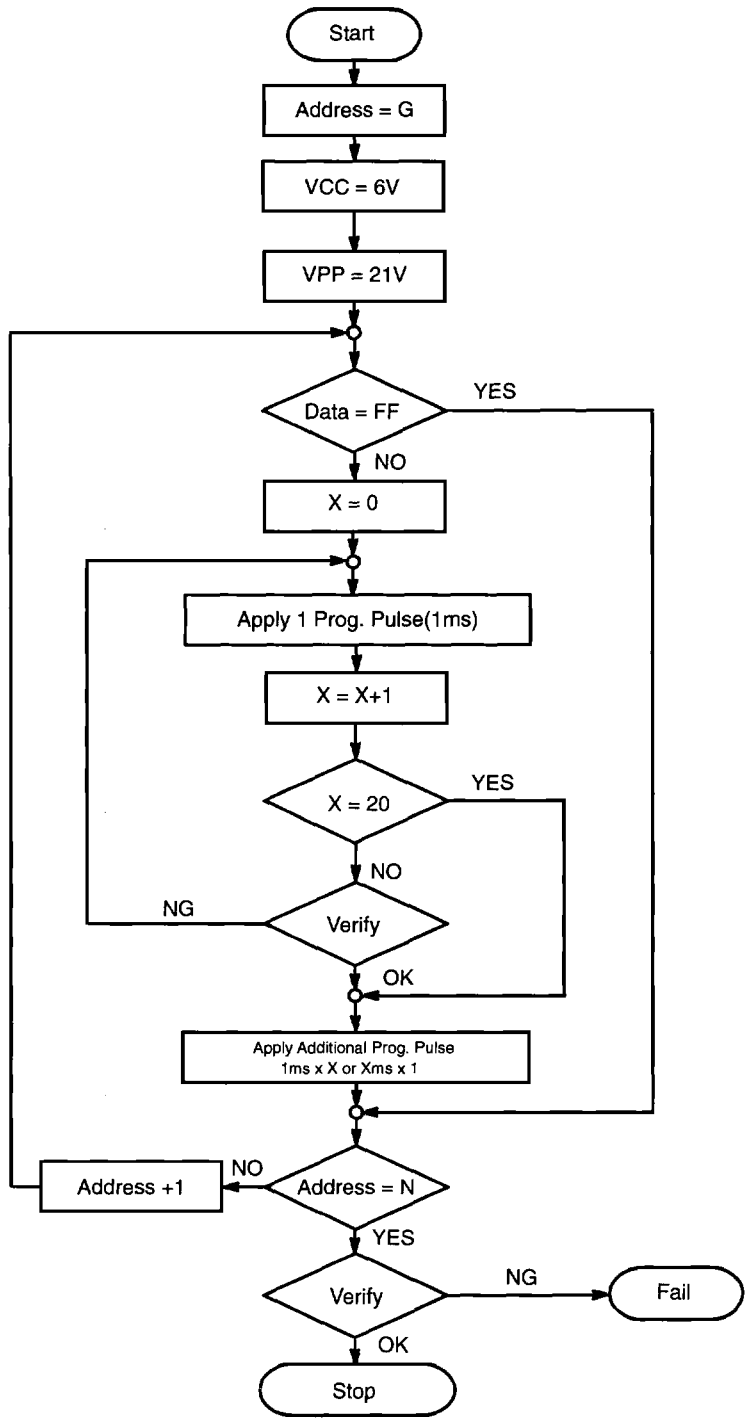
Fig. 17 –QUICK PROGRAMMING FLOW CHART

VCC =6V ±0.25V
VPP = 21V ±0.5V

tpw = 1ms ±50µs
(* = Xms ±5%)

G: Start Address
N: Stop Address

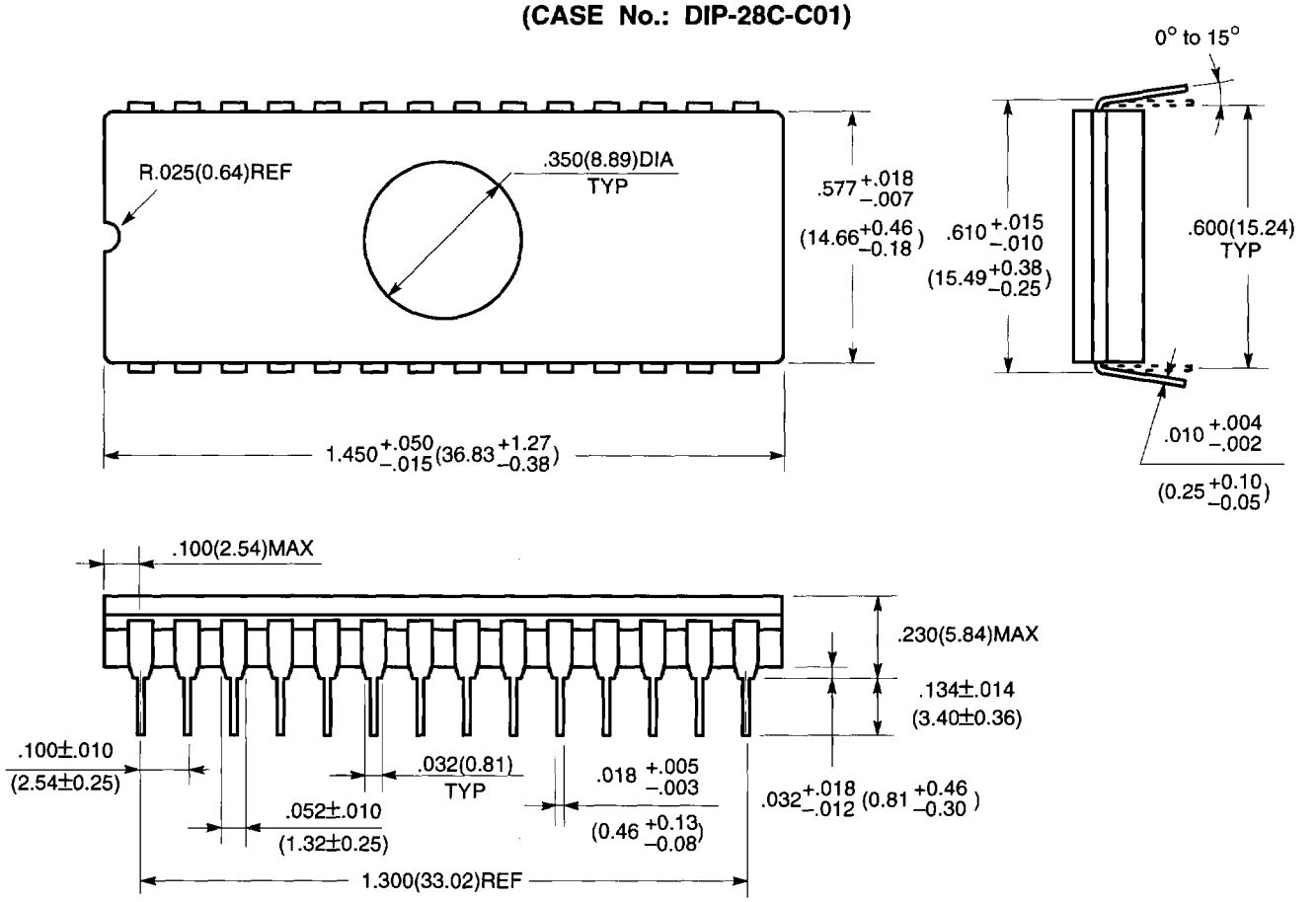
Maximum (40ms +α)/Byte
Minimum (2ms +α)/Byte
(For Example)
64K Bit EPROM
Maximum 320sec. +β
Minimum 16sec. +β



PACKAGE DIMENSIONS

(Suffix: Z)

28-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



Dimensions in
inches (millimeters)