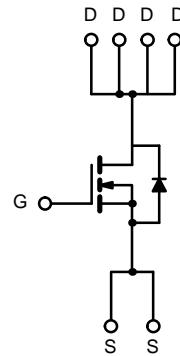
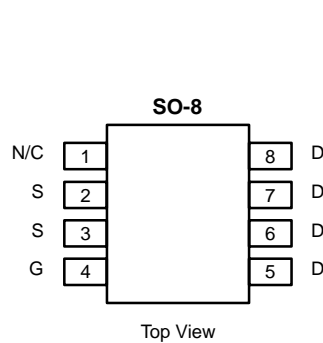


N-Channel Enhancement-Mode MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(ON)} (Ω)	I _D (A)
30	0.030 @ V _{GS} = 10 V	±7.0
	0.040 @ V _{GS} = 5 V	±6.0
	0.050 @ V _{GS} = 4.5 V	±5.4

Recommended upgrade: Si4410DY or Si4936DY
 Lower profile/smaller size—see Si6434DQ


ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	
Continuous Drain Current (T _J = 150°C) ^A	I _D	T _A = 25°C	±7.0
		T _A = 70°C	±5.8
Pulsed Drain Current	I _{DM}	±30	A
Continuous Source Current (Diode Conduction) ^A	I _S	2.8	
Maximum Power Dissipation ^A	P _D	T _A = 25°C	2.5
		T _A = 70°C	1.6
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Maximum Junction-to-Ambient ^A	R _{thJA}	50	°C/W

Notes

A. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70122.
 For SPICE model information via the Worldwide Web: <http://www.siliconix.com/www/product/spice.htm>


SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

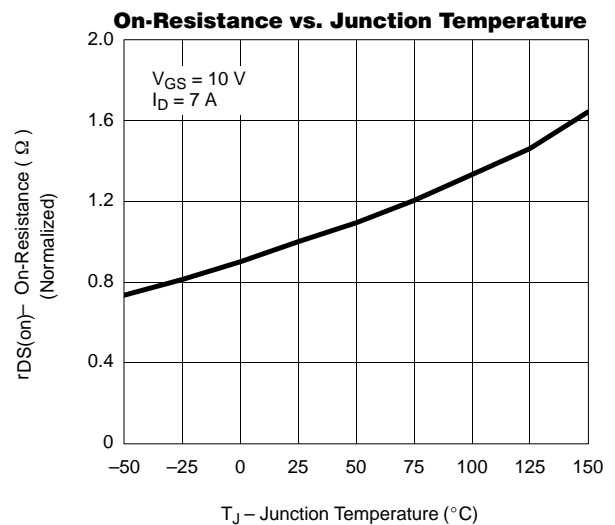
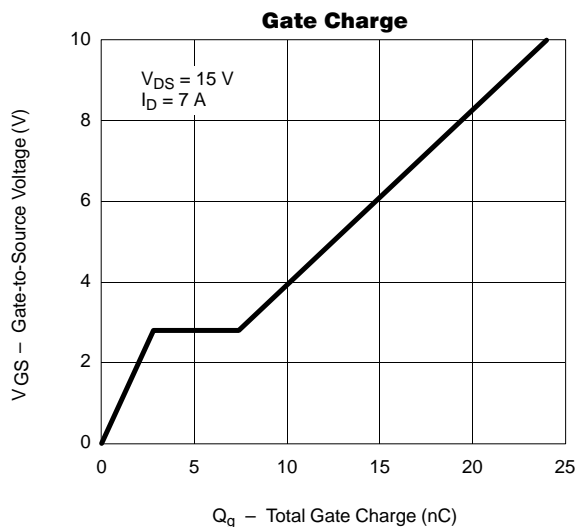
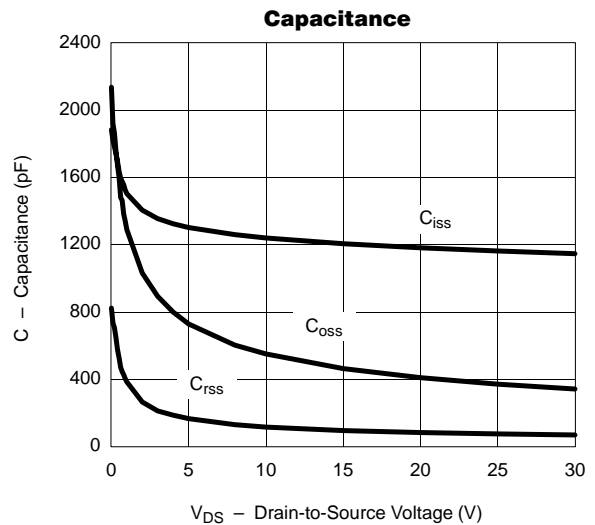
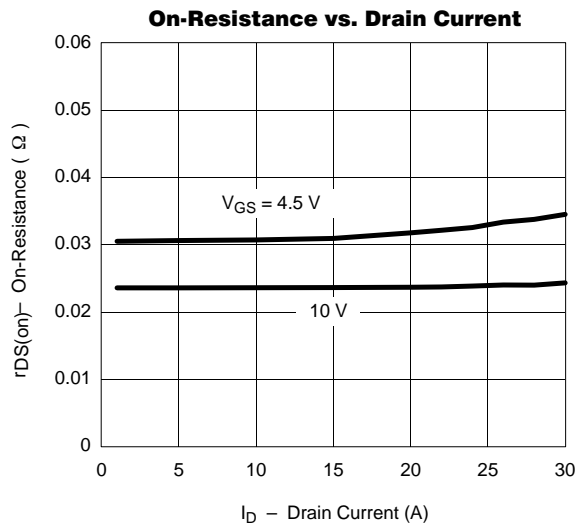
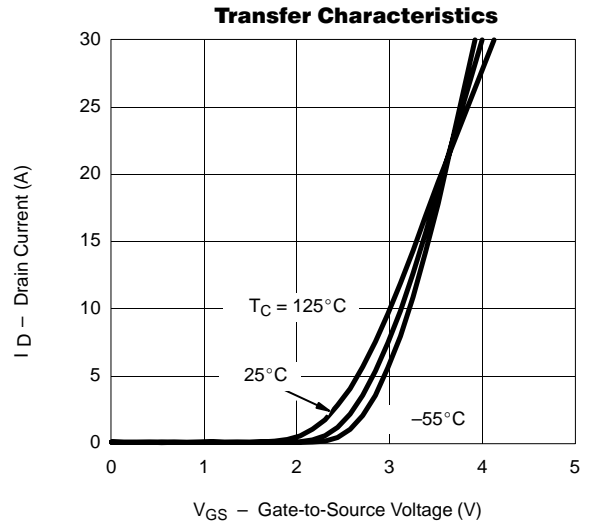
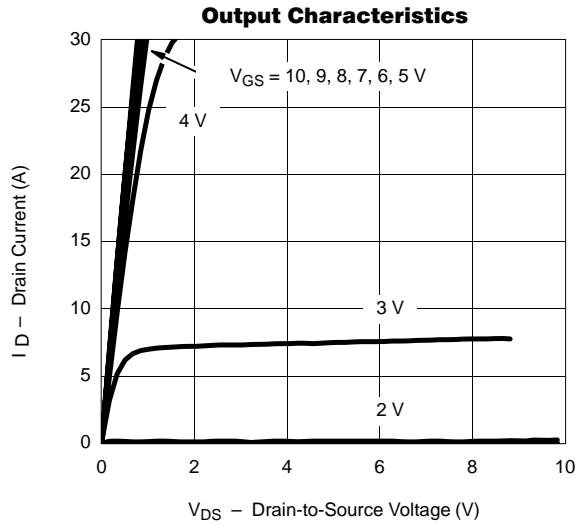
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP ^A	MAX	UNIT
STATIC						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			2	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55°C			25	
On-State Drain Current ^B	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^B	r _{DS(on)}	V _{GS} = 10 V, I _D = 7.0 A		0.024	0.030	Ω
		V _{GS} = 5 V, I _D = 4.0 A		0.030	0.040	
		V _{GS} = 4.5 V, I _D = 3.5 A		0.032	0.050	
Forward Transconductance ^B	g _{fs}	V _{DS} = 15 V, I _D = 7.0 A		15		S
Diode Forward Voltage ^B	V _{SD}	I _S = 2 A, V _{GS} = 0 V		0.72	1.1	V
DYNAMICA						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 2 A		24	50	nC
Gate-Source Charge	Q _{gs}			2.8		
Gate-Drain Charge	Q _{gd}			4.6		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, R _L = 25 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		14	30	ns
Rise Time	t _r			10	60	
Turn-Off Delay Time	t _{d(off)}			46	150	
Fall Time	t _f			17	140	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2 A, di/dt = 100 A/μs		60		

Notes

- A. Guaranteed by design, not subject to production testing.
 B. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)





TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

