MOTOROLA

SN54LS259
SN74LS259

8-BIT ADDRESSABLE LATCH

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable

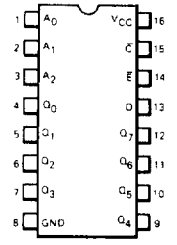
- **SERIAL-TO-PARALLEL CONVERSION**
- **EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**

PIN NAMES

		LOADING (Note a) HIGH	LOW
A_0, A_1, A_2	Address Inputs	0.5 U.L.	0.25 U.L.
D	Data Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{C}$	Clear (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0 to Q_7	Parallel Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

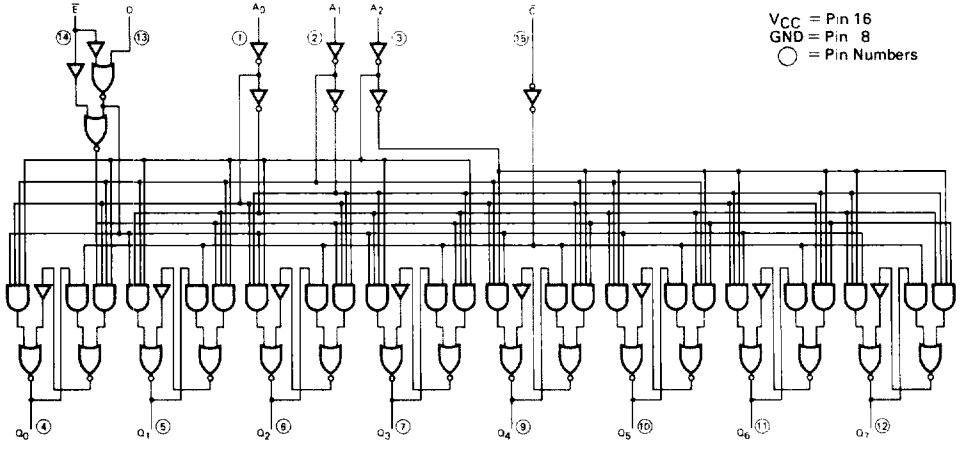
CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

5

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The SN54LS/74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the SN54LS/74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	*Addressable Latch*
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

PRESENT OUTPUT STATES

$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	*Clear*
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	I	I	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					Addressable
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						Latch
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
•	•	•		•					•					
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

5

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54,74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				36	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{PLH}	Turn-Off Delay, Enable to Output		22	35	ns	C_L = 15 pF
t_{PHL}	Turn-On Delay, Enable to Output		15	24	ns	
t_{PLH}	Turn-Off Delay, Data to Output		20	32	ns	
t_{PHL}	Turn-On Delay, Data to Output		13	21	ns	
t_{PLH}	Turn-Off Delay, Address to Output		24	38	ns	
t_{PHL}	Turn-On Delay, Address to Output		18	29	ns	
t_{PHL}	Turn-On Delay, Clear to Output		17	27	ns	

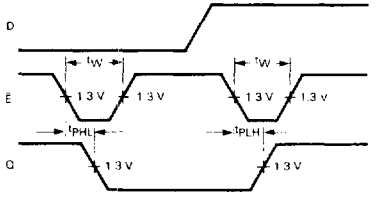
5

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS
		MIN	TYP	MAX	
t_s	Input Setup Time	20			ns
t_W	Pulse Width, Clear or Enable	15			ns
t_h	Hold Time, Data	5.0			ns
t_h	Hold Time, Address	20			ns

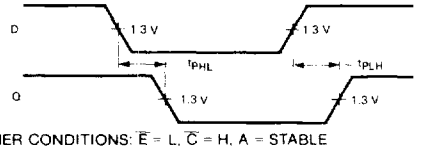
AC WAVEFORMS

Fig. 1 TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



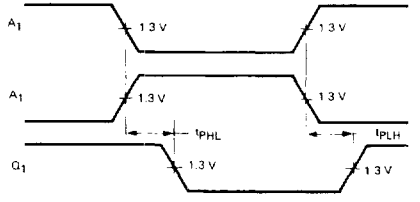
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 2 TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



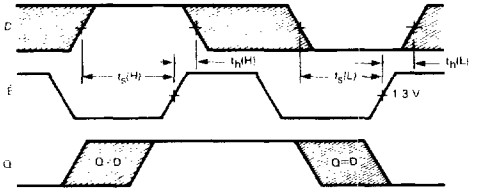
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Fig. 3 TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



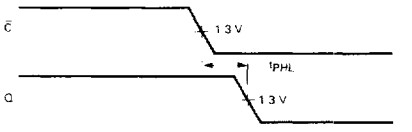
OTHER CONDITIONS $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 SETUP AND HOLD TIME, DATA TO ENABLE



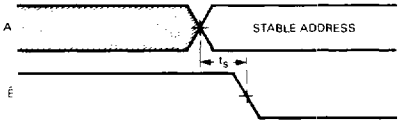
OTHER CONDITIONS $\overline{C}$ = H, A = STABLE

Fig. 5 TURN-ON DELAY, CLEAR TO OUTPUT



OTHER CONDITIONS $\overline{E}$ = H

Fig. 6 SETUP TIME, ADDRESS TO ENABLE (SEE NOTES 1 AND 2)



OTHER CONDITIONS $\overline{C}$ = H

NOTES:
1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

5