PGA100

Digitally-Controlled Programmable Gain/Multiplexed Input OPERATIONAL AMPLIFIER

FEATURES

- HIGH GAIN ACCURACY, ±0.02%, max (B grade)
- LOW NONLINEARITY, ±0.005%, max (B grade)
- FAST SETTLING, 5μsec to 0.01%
- LOW CHANNEL-TO-CHANNEL CROSSTALK, ±0.003%
- INPUT PROTECTION, ±20V, max above $\pm V_{CC}$
- 8 ANALOG INPUT CHANNELS WITH HIGH Z_{IN}, $10^{11}\Omega$
- 8 BINARY GAINS 1, 2, 4, 8, 16, 32, 64, 128 (V/V)
- FULLY MICROPROCESSOR-COMPATIBLE

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- SOFTWARE ERROR CORRECTION
- AUTO-ZEROING CAPABILITY
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- TEST EQUIPMENT
- REMOTE INSTRUMENTATION SYSTEM
- SYSTEM DYNAMIC RANGE AND RESOLUTION IMPROVEMENT

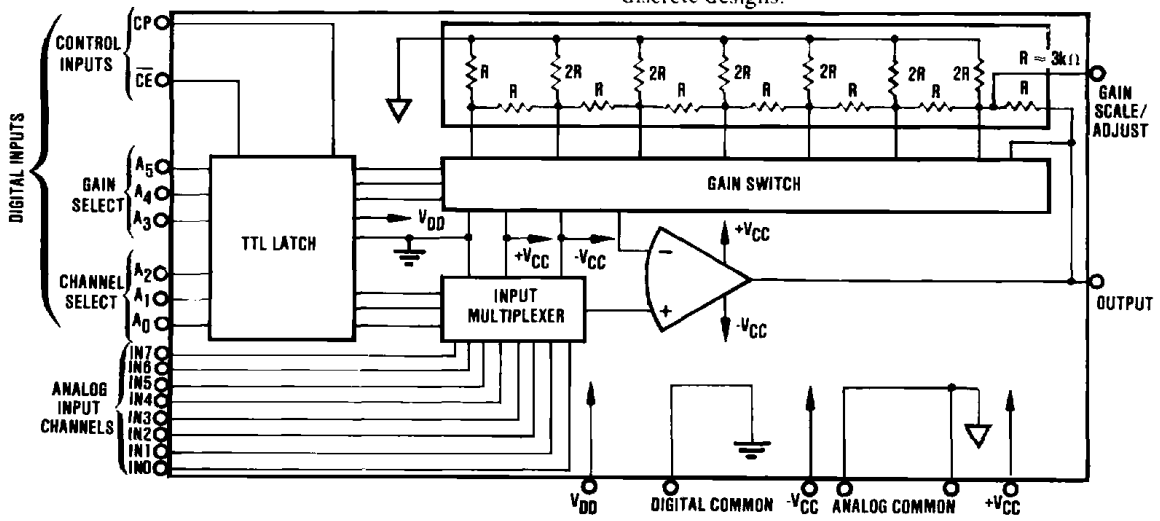
DESCRIPTION

The PGA100 is a precision, digitally-programmable-gain multiplexed-input amplifier. The user can select any one of eight analog input channels simultaneously with any one of eight noninverting binarily weighted gain steps from 1 to 128 (V/V). The digital gain and channel select are latchable for microprocessor interface. Also, the fast 5μsec settling time is ideal for rapid channel scanning in data acquisition systems.

Precision laser-trimming of both offset voltage and gain accuracy, with good temperature tracking of feedback resistor ratios, permits direct use without adjustments. However, hardware or software correction of errors is readily achievable.

In addition, gain scaling to gains other than 1 to 128V/V can easily be accomplished.

Microcircuit construction and the use of laser-trimmed thin-film feedback resistors achieve high accuracy, small size, and low cost not obtained with discrete designs.



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PDS-457B

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, $\pm V_{CC}$ = 15VDC, V_{DD} = +5VDC unless otherwise noted.

PARAMETER	CONDITIONS	PGA100AG			PGA100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GAIN, G								
Inaccuracy(1)	G = 1 to 128, I_o = 1mA		±0.01	±0.05		±0.005	±0.02	%
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±5	±10		•	•	ppm/°C
vs Time			±0.001			•		%/1000 hrs.
Nonlinearity(3)	G = 1 to 128, I_o = 1mA		±0.004	±0.01		±0.002	±0.005	% of FS
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±2	±5		•	•	ppm/°C
vs Time			±0.001			•		%/1000 hrs.
Warm-up Time		1			•			min
RATED OUTPUT								
Voltage	I_o = ±2mA	±10			•			V
Current	V_o = ±10V	±2			•			mA
Output Resistance	G ≤ 128		0.05			•		Ω
Short Circuit Current			±15			•		mA
Capacitive Load Range	Phase Margin ≥ 25°		1000			•		pF
INPUT OFFSET VOLTAGE								
Initial	T_A = +25°C		±0.1	±1		±0.05	±0.5	mV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6			•		µV/°C
vs Supply Voltage	±8VDC ≤ | V_{CC} | ≤ ±18VDC		±10	±80		•	•	µV/V
vs Time			±15			•		µV/mo.
INPUT BIAS CURRENT								
Initial	T_A = +25°C							
"OFF" Channel			±10			•		pA
"ON" Channel			±0.1			•	±1	nA
vs Temperature			Note 4			•		
INPUT DIFFERENCE CURRENT, BETWEEN CHANNELS								
Initial	T_A = +25°C							
"OFF" Channel			±20			•		pA
"ON" Channel			±0.2			•	±2	nA
vs Temperature			Note 4			•		
ANALOG INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±(|V_{CC}|+20)			•	V
Input Voltage Range	Linear operation	±10			•			V
Input Impedance								
"OFF" Channel			10^{12} || 5			•		Ω || pF
"ON" Channel			10^{11} || 25			•		Ω || pF
INPUT NOISE								
Voltage Noise Density	f_o = 1Hz		200			•		nV/√Hz
	f_o = 10Hz		60			•		nV/√Hz
	f_o = 100Hz		25			•		nV/√Hz
	f_o = 1kHz		18			•		nV/√Hz
	f_o = 10kHz		18			•		nV/√Hz
	f_o = 100kHz		18			•		nV/√Hz
Voltage Noise	f_B = 0.1Hz to 10Hz		2.6			•		µV, p-p
Current Noise Density	f_o = 0.1Hz thru 8kHz		6			•		fA/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		115			•		fA, p-p
DYNAMIC RESPONSE								
Gain Bandwidth Product			5			•		MHz
Full Power Bandwidth	G = 1, V_o = 20V, p-p, R_L = 5kΩ		220		80	•		kHz
Slew Rate	G = 1, V_o = ±10V, R_L = 5kΩ		14		5	•		V/µsec
Settling Time(5)	G = 1, V_o = ±10V, R_L = 5kΩ							
ε = 1%			2.5			•		µsec
ε = 0.1%			3			•		µsec
ε = 0.01%			5			•		µsec
Rise Time	10% to 90%, small signal		70			•		nsec
Phase Margin	G = 1, R_L = 5kΩ		60			•		Degrees
Overload Recovery (6)	G = 1, 50% overdrive		2			•		µsec
Crosstalk, RTI(5)(7)	20V, p-p, 1kHz sine, R_S = 1kΩ on all OFF channels		±0.003			•		%
DIGITAL INPUT(8)								
Input "Low" Threshold, V_{IL}				0.8			•	V
Input "High" Threshold, V_{IH}		2.0			•			V
f_{max}, Maximum Clock Frequency		30			•			MHz
t_{WL}, Clock Pulse Width (Low)	Figure 1	20			•			nsec
t_{s_1}, Setup Time (Data to CP)	Figure 1	20			•			nsec
t_{h_1}, Hold Time (Data to CP)	Figure 1	5			•			nsec
t_{s_2}, Setup Time ($\overline{CE}$ to CP)	Figure 1	25			•			nsec
t_{h_2}, Hold Time ($\overline{CE}$ to CP)	Figure 1	5			•			nsec

ELECTRICAL (CONT)

PARAMETER	CONDITIONS	PGA100AG MIN	PGA100AG TYP	PGA100AG MAX	PGA100BG MIN	PGA100BG TYP	PGA100BG MAX	UNITS
ANALOG SUPPLY								
Rated Voltage	Derated performance	±8	±15	±18				VDC
Voltage Range								V
Positive Quiescent Current			+20	+27		-15	+20	mA
Negative Quiescent Current			-10	-16		-7.5	-12	mA
DIGITAL SUPPLY								
Rated Voltage			+5					VDC
Voltage Range		+4.75		+5.25				V
Quiescent Current	V_{DD} = +5.25V		15	27				mA
TEMPERATURE RANGE								
Specification	Derated performance	-25		+85				°C
Operating		-55		+125				°C
Storage		-55		+125				°C

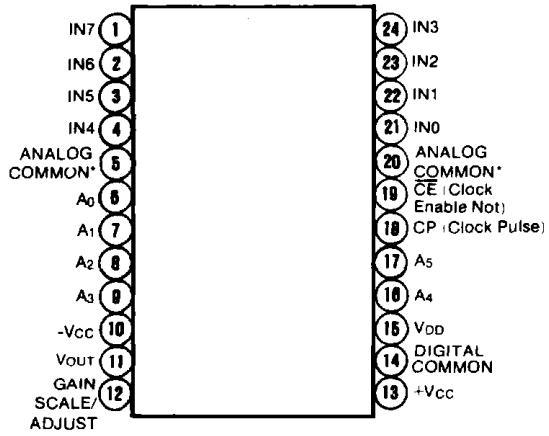
*Specifications same as PGA100AG.

NOTES:
1. Inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero.
2. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
3. Nonlinearity is the maximum peak deviation from a "best straight line" (curve fitting on input-output graph) expressed as a percent of the full scale peak-to-peak output. Gain constant, V_{OUT} ranges from -10V to +10V.
4. Doubles approximately every 10°C.
5. See Typical Performance Curves.
6. Time required for the output to return from saturation to linear operation following the removal of an input overdrive signal.
7. Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the signal applied to all OFF channels.
8. All digital inputs are one 74LSTTL load.

ABSOLUTE MAXIMUM RATINGS

Analog Supply	±18V
Digital Supply	+7V
Input Voltage Range, Analog	±(|V_{CC}| +20)V
Input Voltage Range, Digital	+7V
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

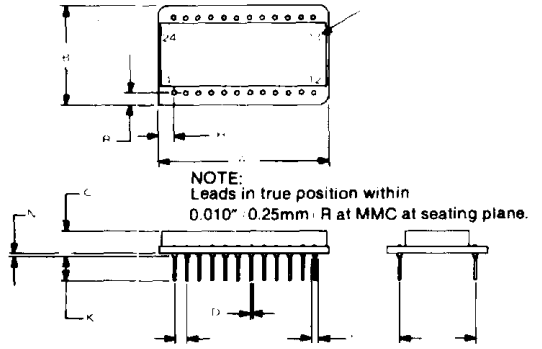
PIN DESIGNATIONS



*Connected internally. Use pin 20 as the primary analog common.

MECHANICAL

Pin numbers shown for reference only.
Numbers may not be marked on package.



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 6.3 grams (0.225 oz.)
HERMETICITY: Conform to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
E	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

ORDERING INFORMATION

Model	Package	Temperature Range
PGA100AG	Ceramic	-25°C to +85°C
PGA100BG	Ceramic	-25°C to +85°C

BURN-IN SCREENING OPTION
See text for details.

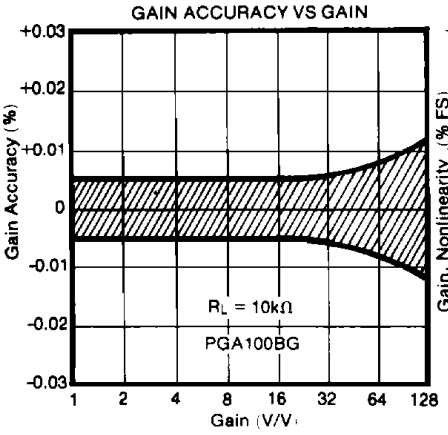
Model	Package	Burn-In Temp. (160h)(1)
PGA100AG-BI	Ceramic	+125°C
PGA100BG-BI	Ceramic	+125°C

NOTE: (1) Or equivalent combination. See text.

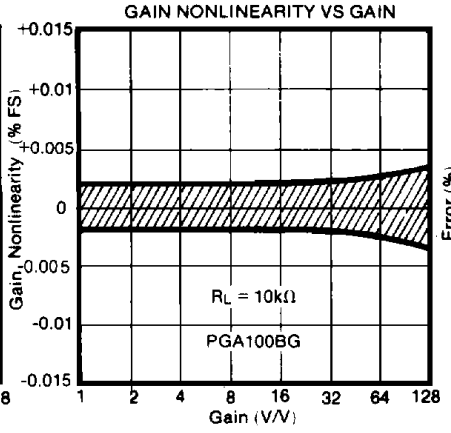
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC, unless otherwise noted.)

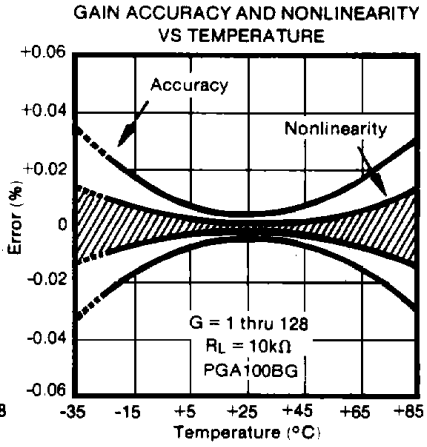
GAIN ACCURACY VS GAIN



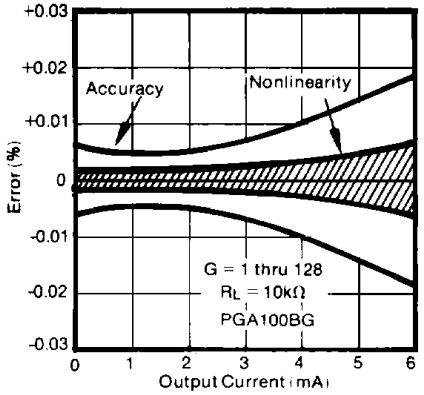
GAIN NONLINEARITY VS GAIN



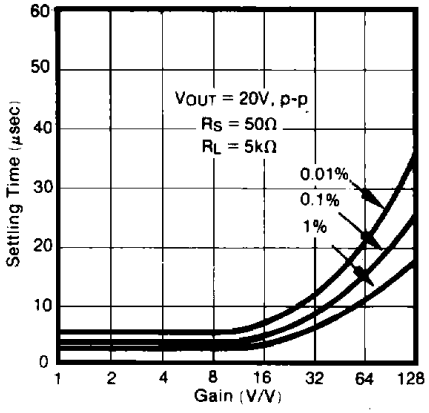
GAIN ACCURACY AND NONLINEARITY VS TEMPERATURE



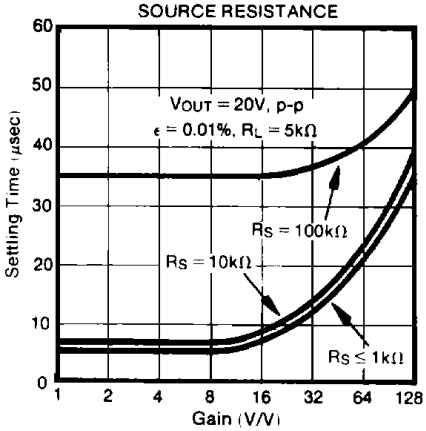
GAIN ACCURACY AND NONLINEARITY VS OUTPUT CURRENT



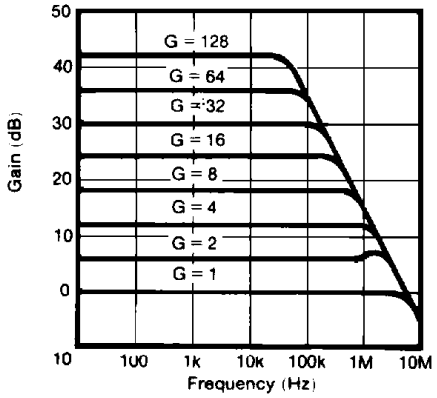
SETTLING TIME VS GAIN



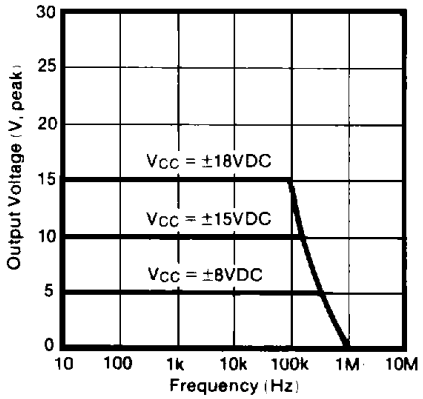
SETTLING TIME VS GAIN AND SOURCE RESISTANCE



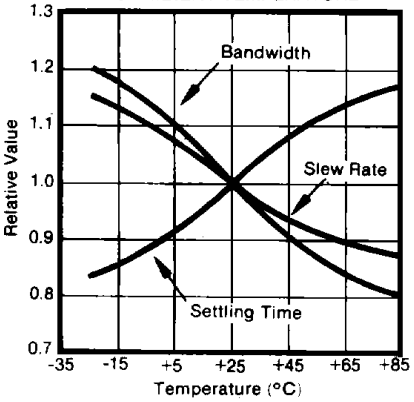
SMALL SIGNAL FREQUENCY RESPONSE



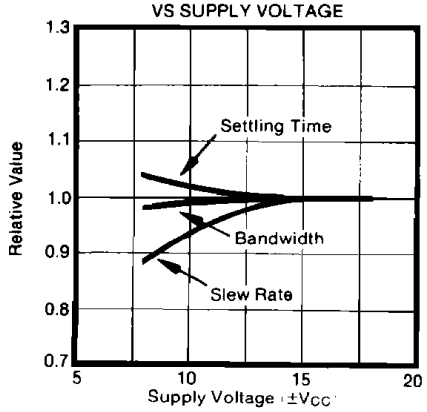
LARGE SIGNAL OUTPUT VOLTAGE VS FREQUENCY



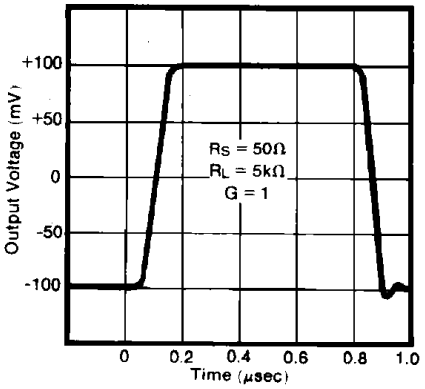
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



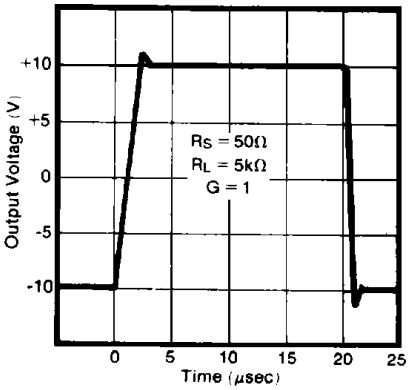
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



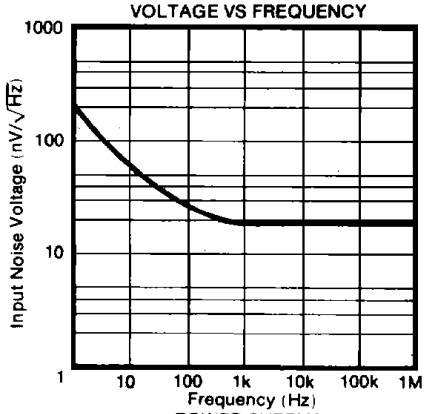
SMALL SIGNAL TRANSIENT RESPONSE



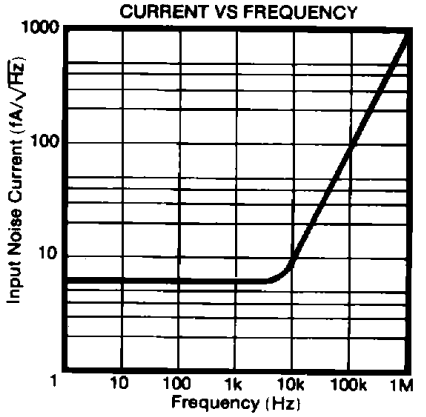
LARGE SIGNAL TRANSIENT RESPONSE



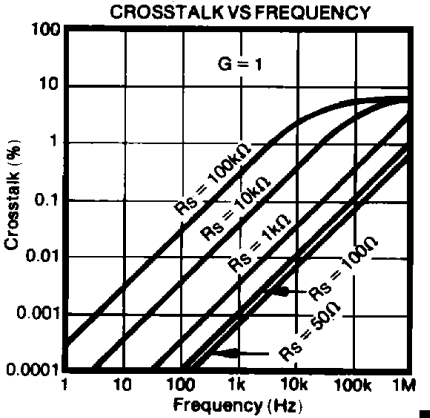
INPUT NOISE VOLTAGE VS FREQUENCY



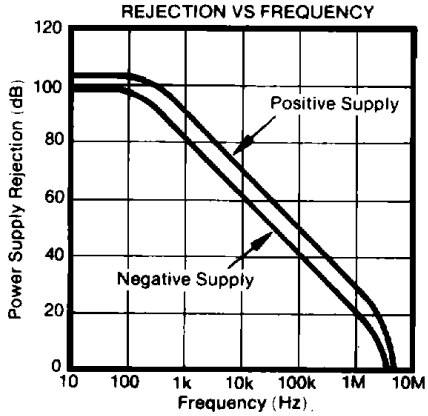
INPUT NOISE CURRENT VS FREQUENCY



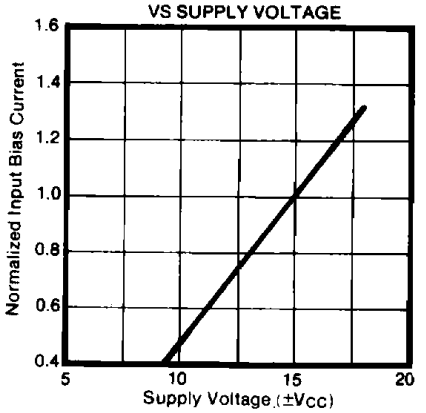
CHANNEL-TO-CHANNEL CROSSTALK VS FREQUENCY



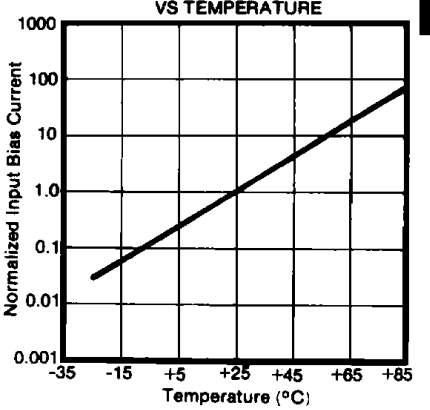
POWER SUPPLY REJECTION VS FREQUENCY



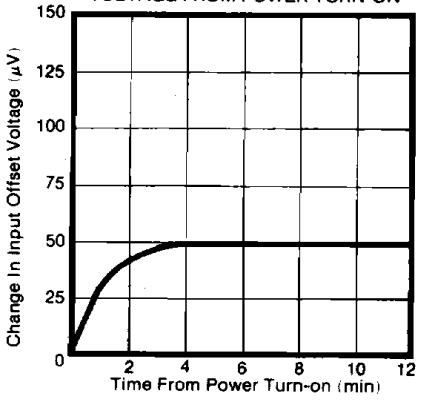
INPUT BIAS CURRENT VS SUPPLY VOLTAGE



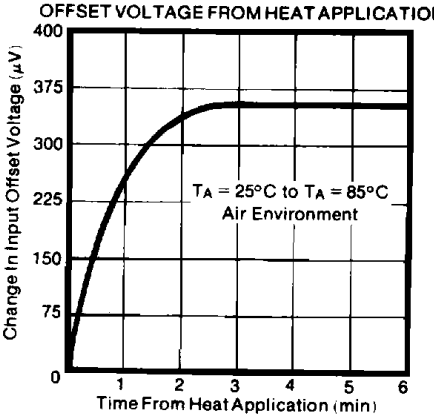
INPUT BIAS CURRENT VS TEMPERATURE



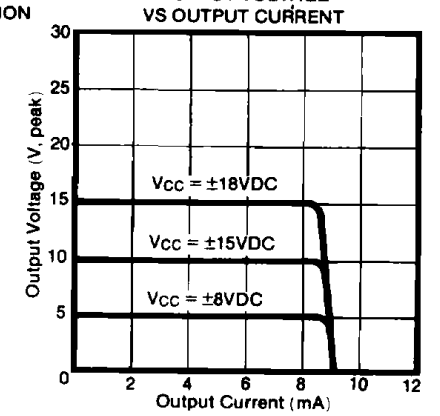
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



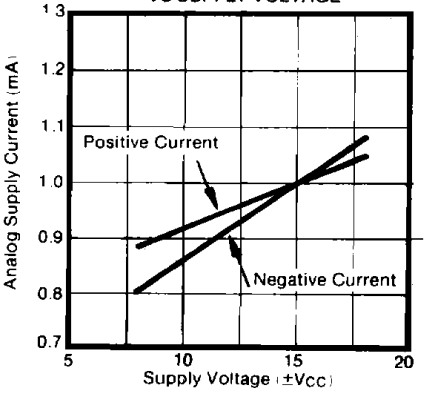
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



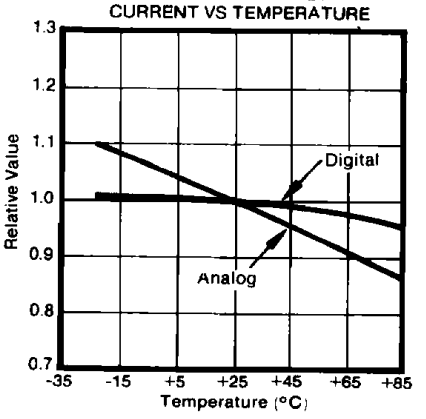
OUTPUT VOLTAGE VS OUTPUT CURRENT



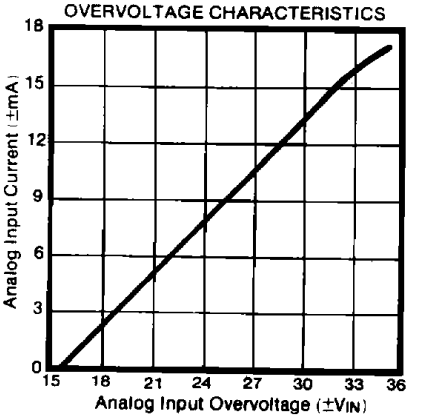
ANALOG SUPPLY CURRENT VS SUPPLY VOLTAGE



QUIESCENT SUPPLY CURRENT VS TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



BURN-IN SCREENING

Burn-in screening is an option available for the PGA100. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

DISCUSSION OF PERFORMANCE

The PGA100 is a self-contained programmable-gain amplifier whose gain can be changed in 8 binarily weighted steps from 1 to 128 or as scaled externally through the gain scale adjust pin. The gain control is accomplished by the gain switch (break-before-make) whose position is determined by the 3-bit TTL address, A_3, A_4, and A_5. When selected, 1 of 8 positions connects the thin-film resistor network to the feedback loop of the op amp. This establishes the desired gain. (See Installation and Operating Instructions for gain scaling.)

Similarly, the 8 analog input channels are switched by the input multiplexer (break-before-make) whose position is determined by the 3-bit TTL address, A_0, A_1, and A_2. Gain and channel selection appear in Table I. 64-channel gain combinations are possible.

The digital inputs are latched by the positive transition of the clock pulse, pin 18, when the clock enable, pin 19, is low. The relative set up and holding times specified in the Electrical Specifications are shown in Figure 1. The internal latch is similar to the industry standard 74LS378. Figure 2 shows a timing diagram for selected addresses indicating: the enable function, changing channel and gain, changing channel constant gain, and constant channel changing gain.

TABLE I. Gain and Channel Select Truth Table.

GAIN SELECT			GAIN	CHANNEL SELECT			CHANNEL
A_5	A_4	A_3		A_2	A_1	A_0	
0	0	0	1	0	0	0	IN0
0	0	1	2	0	0	1	IN1
0	1	0	4	0	1	0	IN2
0	1	1	8	0	1	1	IN3
1	0	0	16	1	0	0	IN4
1	0	1	32	1	0	1	IN5
1	1	0	64	1	1	0	IN6
1	1	1	128	1	1	1	IN7

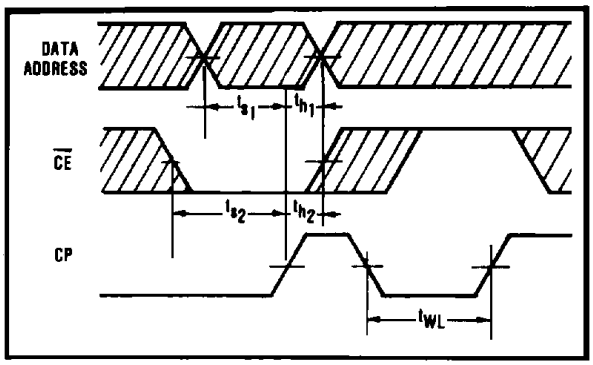


FIGURE 1. Data Address and Clock Enable Setup and Hold Times.

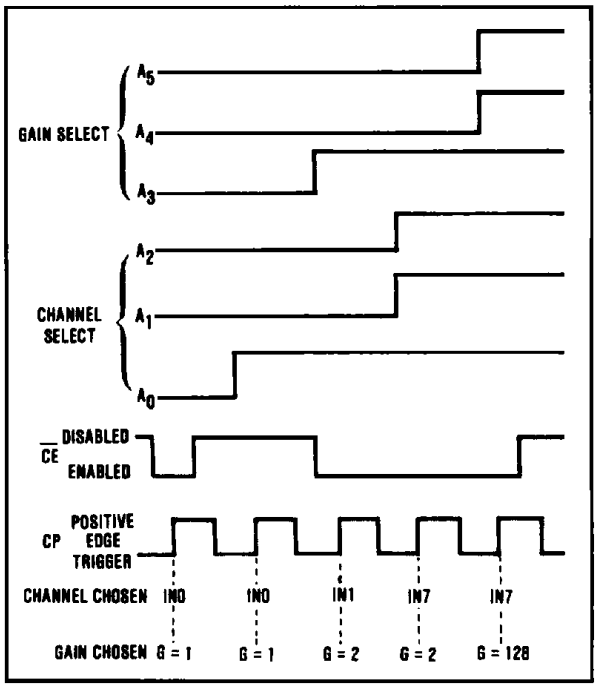


FIGURE 2. Timing Diagram for Selected Addresses.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

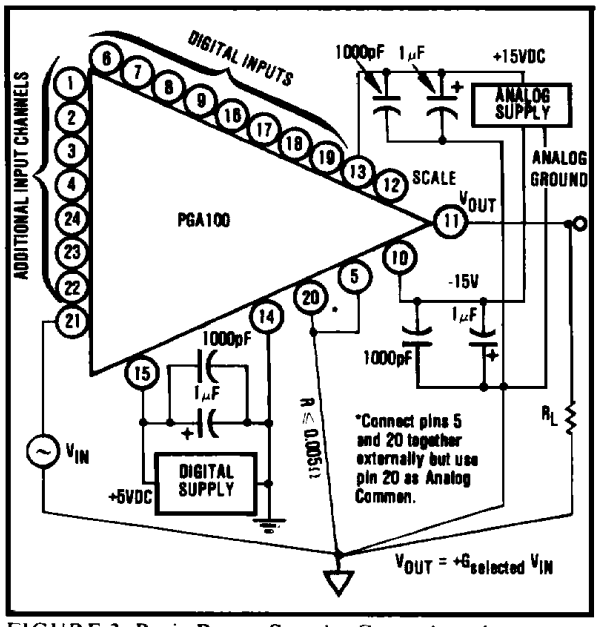


FIGURE 3. Basic Power Supply, Ground, and Signal Connections.

Figure 3 shows the proper analog and digital power supply connections. The supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. To avoid gain errors connect grounds as indicated being sure to minimize ground resistance. Note that a resistance of greater than

0.005Ω in series with the analog common will degrade the specified gain accuracy. IMPORTANT: Normally the digital ground is brought in from the digital power supply on a separate line. However, the analog and digital commons must be connected together somewhere in the system.

OPTIONAL GAIN SCALE/ADJUST

The gain scale/adjust pin is shown in Figure 4. When no connection is made, gains appear as in Table I. At least two functions can be performed. First, the gain range can be scaled to gains other than 1 to 128, for example, 1 to 100 or 1 to 1024. Gain steps, however, retain binary weighting. Some examples are: (1, 1, 2, 4, 8, 16, 32, 64 with pins 11 and 12 connected together), (1, 1.5625, 3.125, 6.25, 12.5, 25, 50, 100), (1, 12.5, 25, 50, 100, 200, 400, 800), and (1, 16, 32, 64, 128, 256, 512, 1024). Scaling is accomplished by using a potentiometer, R_1, shown in Figure 4. Be certain to use a potentiometer of good mechanical and thermal stability. Additional gain drift with temperature should be minimal since it depends on the thermal tracking of the resistance ratio, R_A to R_B, set by the potentiometer.

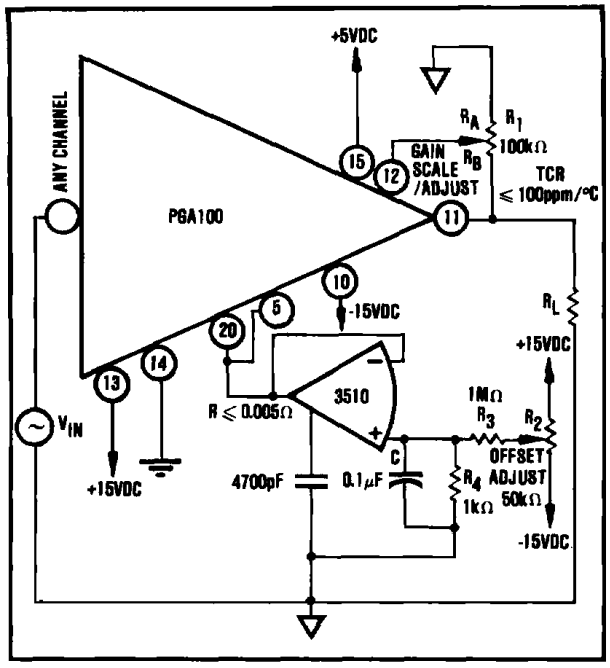


FIGURE 4. External Gain and Offset Adjustment.

Second, the gain inaccuracy, remaining after laser trimming at the factory, can be adjusted to zero at any gain other than unity. To improve resolution and limit adjustment range, a resistor may be added in series with the wiper of the potentiometer and pin 12. This will, however, increase gain drift. Figure 5 shows the effect of gain adjustment. R_1 does not affect gain linearity.

OPTIONAL OFFSET ADJUSTMENT

Figure 4 also illustrates a technique for offset adjustment. This adjustment has no effect at unity gain. R_2 will trim the offset to zero and have neglible effect on the gain accuracy. For best results, trim the offset at the highest

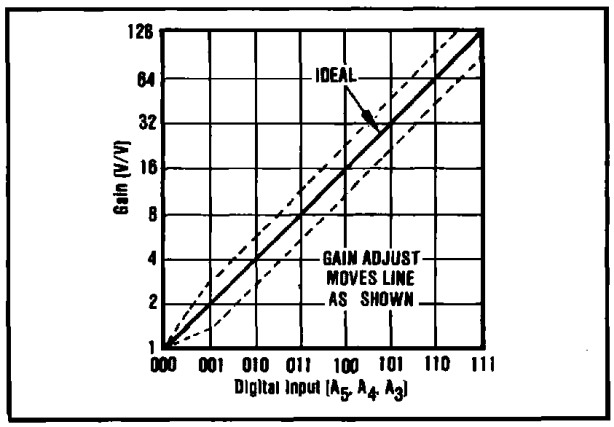


FIGURE 5. Effect of Gain Adjustment.

gain. If R_3 is made smaller, output offsetting can be accomplished. This can be used to introduce an intentional DC voltage at the output. The external amplifier used will add to the input noise, therefore, use one with a noise level of at least three times lower than that specified for the PGA100.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PGA100. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate analog and digital runs to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration as shown in Figure 3. Analog and digital commons must be connected at some point in the system to insure proper operation.

GAIN INACCURACY AND NONLINEARITY

As shown in Figure 3, connect pins 5 and 20 directly together at the unit and use pin 20 as the primary analog common. Ground resistance in series with pin 20 also appears in series with the internal gain-setting resistors and will decrease the magnitude of all gains except unity. The resulting accuracy error varies nonlinearly with the gain selected and therefore cannot be externally adjusted to zero for more than one gain at a time. Gain linearity is not affected by external ground resistance (see Performance Curves.)

CROSSTALK

Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the input signal applied to all OFF channels. For example, the 0.003% specification indicates that 0.6mV, p-p, out of a 20V, p-p, 1kHz sine wave (applied to 7 OFF channels) will appear at the noninverting input of the internal op amp. Note that crosstalk increases with high frequencies due to the capacitive coupling between ON and OFF channels. It also increases with greater source resistance. However, because both the input signal and crosstalk noise are amplified equally, the resulting output signal-to-noise

ratio is independent of gain. Unused input channels should be grounded in order to reduce crosstalk and extraneous noise pickup. (See Performance Curves.)

SETTLING TIME

Settling time is the time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is a very important consideration since this will be the limiting parameter in determining the maximum channel scanning or throughput rate. The PGA100 specification includes the effects of both the multiplexer and amplifier. Note that settling time increases with increasing source resistance and gain. Minimum settling time is achieved by choosing a low source resistance, for example, $R_S \leqslant 10k\Omega$ and gains $\leqslant 16$. (See Performance Curves.)

INPUT OVERVOLTAGE PROTECTION

The PGA100 provides input overvoltage protection of 20V in excess of either power supply voltage expressed as $\pm(|V_{CC}|+20)$. This is achieved in the dielectrically isolated analog multiplexer which will withstand overvoltage even when the power supplies are off. As a consequence the PGA100 is protected against high input levels and brief transient spikes of up to several hundred volts that can result from signals originating from outside the system. (See Performance Curves.)

TYPICAL APPLICATIONS

The PGA100 is ideal for a variety of applications, especially where low channel-to-channel crosstalk is required. In many applications the PGA100 will not require trimming of offset and gain errors. However, these can be minimized utilizing hardware or software error correction techniques. Figures 6 and 7 show applications of the PGA100 separately and in a data acquisition system.

Figure 7 shows a Data Acquisition System. In this system the PGA100 allows the user to deal with signals of wide dynamic range while maintaining high system resolution. For example: When used with a 12-bit A/D converter in a "floating point" system, the 2^7 gain range of the PGA100 plus the 2^{12} range of the converter produces a total system resolution of 2^{19} (524,000 to 1).

Also the user can modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated amplifiers are not required for various input channels, the PGA100 also saves space and overall system costs. Software correction virtually eliminates system offset and gain errors over both time and temperature.

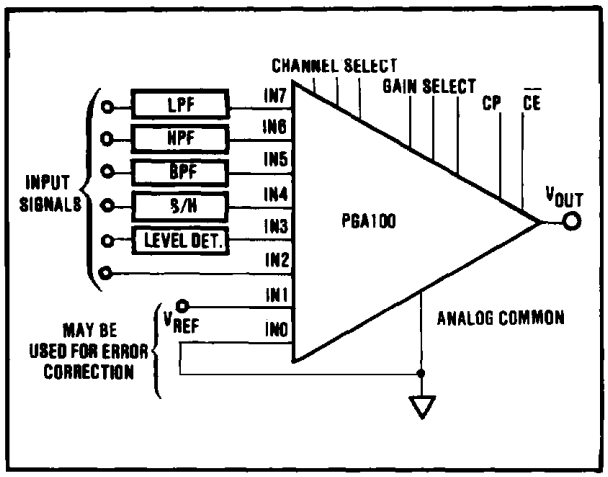


FIGURE 6. Digitally Selectable Function Amplifier.

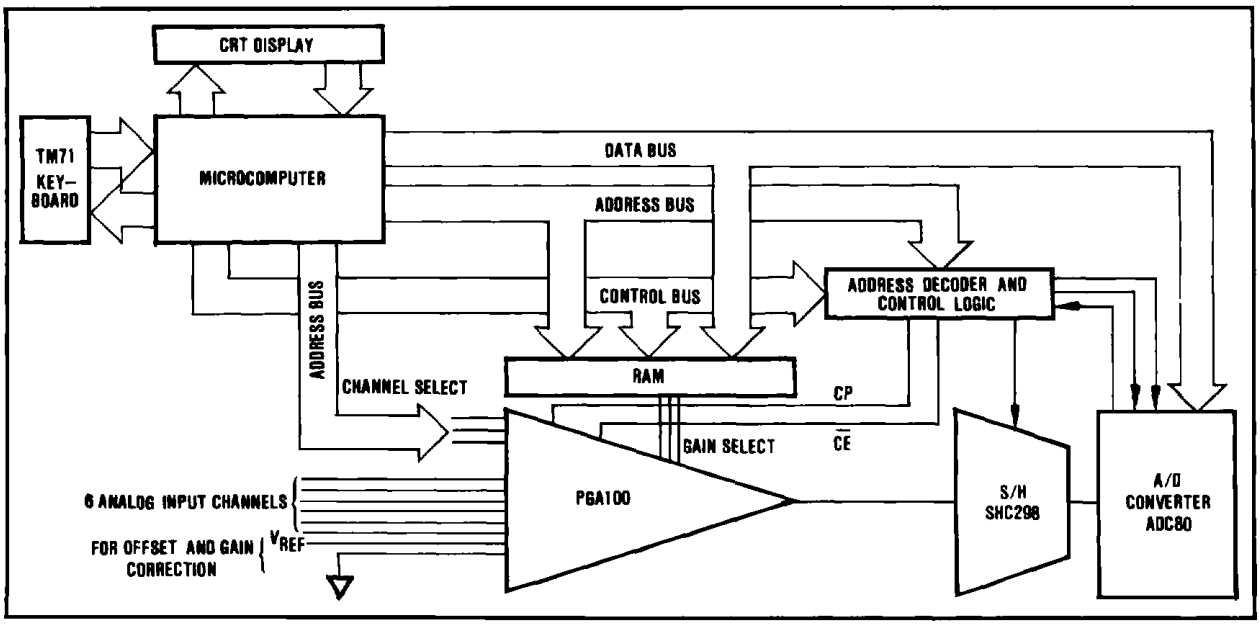


FIGURE 7. Use of PGA100 in a Data Acquisition System with Software Auto-zero and Gain Calibration.