

System Reset Monolithic IC PST572

Outline

This IC functions in a variety of CPU systems and other logic systems, to detect power supply voltage and reset the system accurately when power is turned on or interrupted. This ultra-low current consumption low reset type system reset IC was developed using high resistance process and low current circuit design technology.

Features

1. Ultra-low current consumption
2. Low operating limit voltage
3. Output current high for ON
4. Hysteresis voltage provided in detection voltage
5. 10 ranks of detection voltage

$I_{CCH}=1\mu A$ typ. $I_{CCL}=180\mu A$ typ.
 0.65V typ.
 30mA typ.
 50mV typ.

PST572 C : 4.5V typ.	H : 3.1V typ.
D : 4.2V typ.	I : 2.9V typ.
E : 3.9V typ.	J : 2.7V typ.
F : 3.6V typ.	K : 2.5V typ.
G : 3.3V typ.	L : 2.3V typ.

Package

MMP-3A (PST572□M)

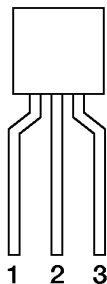
TO-92A (PST572□)

*□ contains detection voltage rank.

Applications

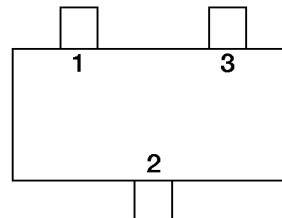
1. Reset circuits in microcomputers, CPUs and MPUs.
2. Logic circuit reset circuits.
3. Battery voltage check circuits.
4. Back-up power supply switching circuits.
5. Level detection circuits.

Pin Assignment



TO-92A

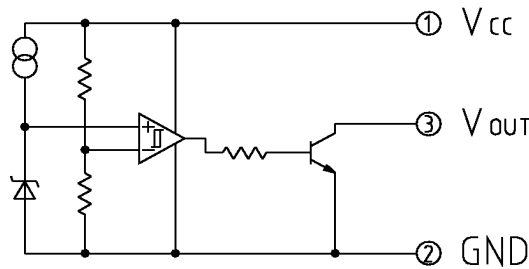
1	V _{CC}
2	GND
3	V _{OUT}



MMP-3A

1	V _{CC}
2	GND
3	V _{OUT}

Equivalent Circuit Diagram



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC} max.	-0.3~10	V
Allowable loss	P _d	200(MMP-3A) 300(TO-92A)	mW

Electrical Characteristics (Ta=25°C)(Except where noted otherwise, resistance unit is Ω)

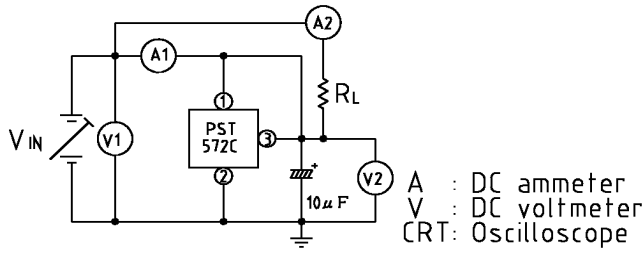
Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units	
Detection voltage	V _s	1	R _L =470 V _{OL} ≤ 0.4V V _{CC} =H→L	PST572C	4.3	4.5	4.7	V
				PST572D	4.0	4.2	4.4	
				PST572E	3.7	3.9	4.1	
				PST572F	3.4	3.6	3.8	
				PST572G	3.1	3.3	3.5	
				PST572H	2.9	3.1	3.3	
				PST572I	2.75	2.90	3.05	
				PST572J	2.55	2.70	2.85	
				PST572K	2.35	2.50	2.65	
				PST572L	2.15	2.30	2.45	
Hysteresis voltage	ΔV _s	1	R _L =470, V _{CC} =L→H→L	25	50	100	mV	
Detection voltage temperature coefficient	V _s /ΔT	1	R _L =470, Ta= -20°C~+75°C		±0.01		%/°C	
Low-level output voltage	V _{OL}	1	V _{CC} =V _s min.-0.05V, R _L =470		0.1	0.4	V	
Output leakage current	I _{OH}	1	V _{CC} =10.0V			±0.1	μA	
Circuit current while on	V _{CC} L	1	V _{CC} =V _s min.-0.05V, R _L =∞		180	300	μA	
Circuit current while off	I _{CC} H	1	V _{CC} =V _s typ./0.85V, R _L =∞		1.0	1.8	μA	
"H"transport delay time	tpLH	2	R _L =4.7kΩ, C _L =100pF *1		30	60	μS	
"L"transport delay time	tpHL	2	R _L =4.7kΩ, C _L =100pF *1		7	20	μS	
Operation limit voltage	V _{op} L	1	R _L =4.7kΩ, V _{OL} ≤ 0.4V		0.65	0.85	V	
Output current while on I	I _{OL} I	1	V _{CC} =V _s min.-0.05V, R _L =0	8	30		mA	
Output current while on II	I _{OL} II	1	Ta=-20°C~+75°C *2	5			mA	

*1 : tpLH : V_{CC}=(V_s typ.-0.4V)→(V_s typ.+0.4V), tpHL : V_{CC}=(V_s typ.+0.4V)→(V_s typ.-0.4V)

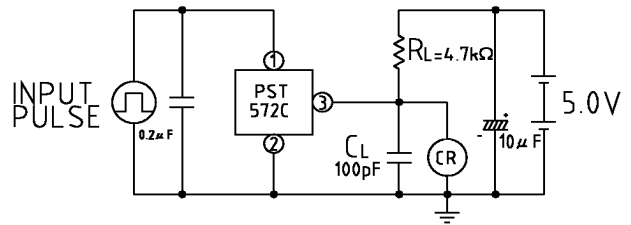
*2 : V_{CC}=V_s min.-0.15V

Measuring Circuit

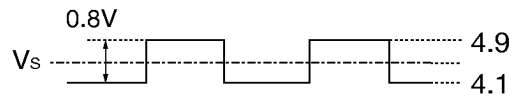
[1]



[2]



Input pulse

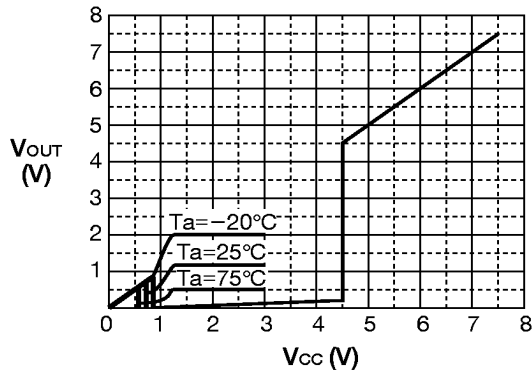


0V

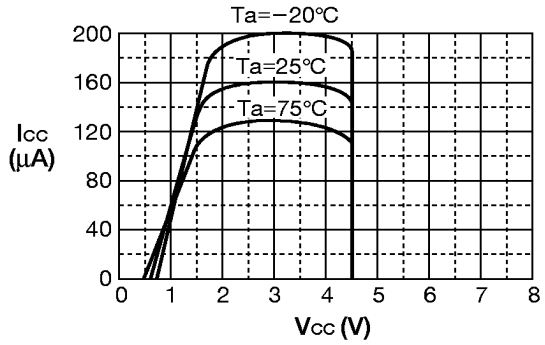
Note: Input model is an example for PST572C.

Characteristics (Example: PST572C)

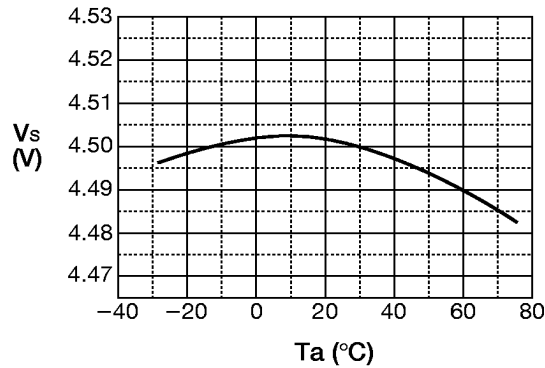
V_{CC} vs. V_{OUT}



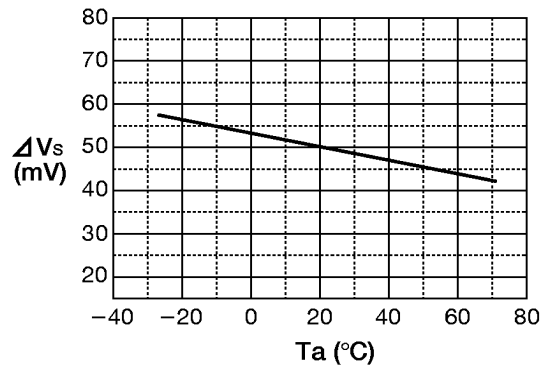
V_{CC} vs. I_{CC}



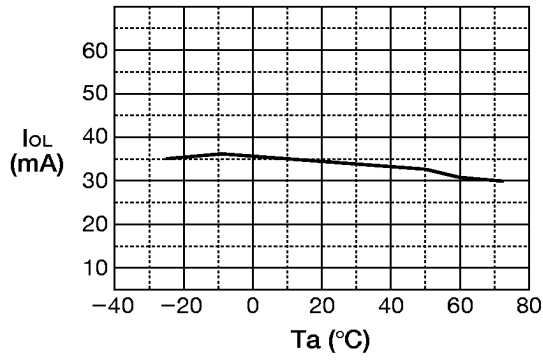
V_s vs. T_a



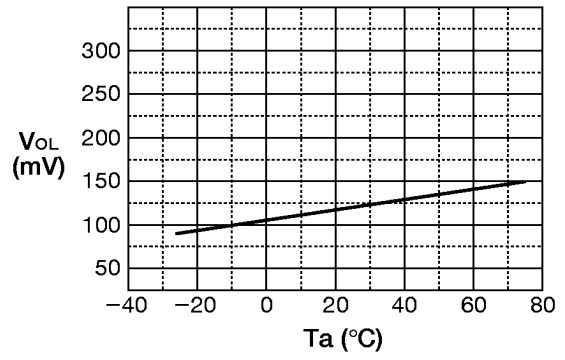
ΔV_s vs. T_a



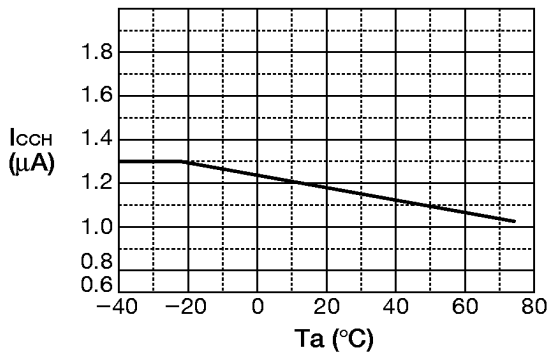
IoL vs. Ta



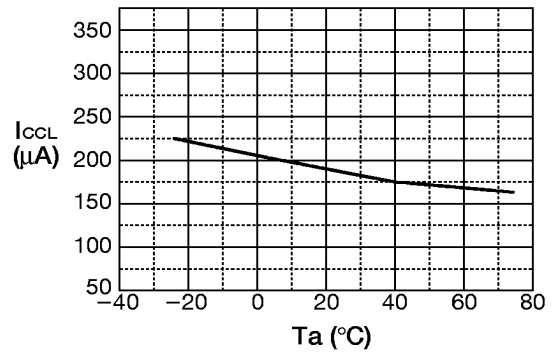
VoL vs. Ta



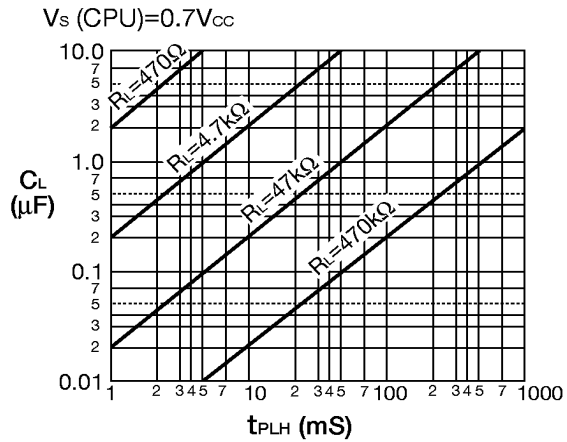
IcCH vs. Ta



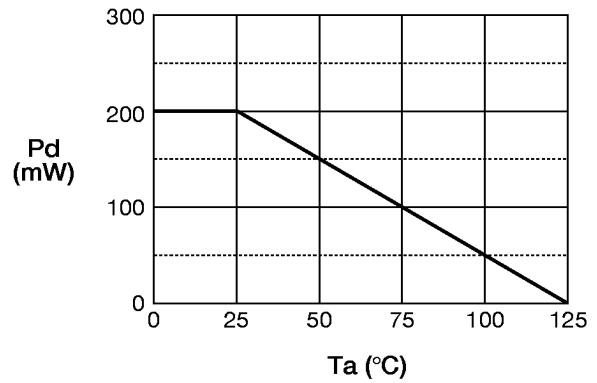
IcCL vs. Ta



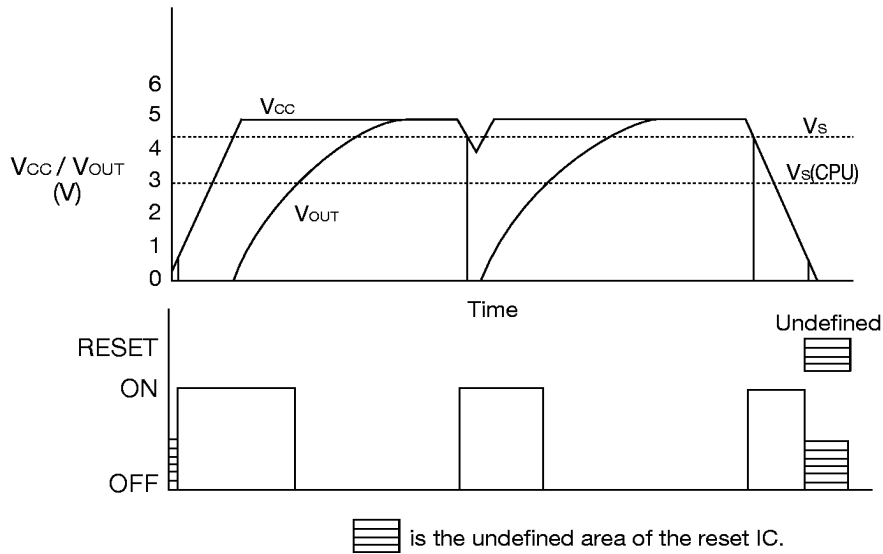
CL(RL) vs. tpLH



Pd vs. Ta

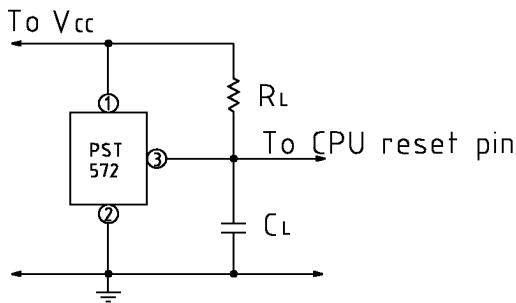


Timing Chart



Application Circuits

1. Normal hard reset



Delay time (t_{pLH})

$$\approx C_L \times R_L \times \left[\ln \frac{V_{CC}}{V_{CC} - (V_s \text{ cpu} + 0.2)} \right] + 0.025(\text{mS})$$

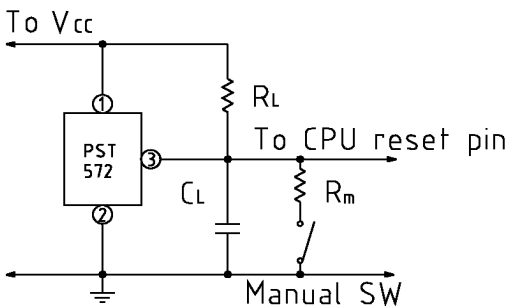
C_L : μF · $V_s \text{ cpu}$: Reset threshold voltage of CPU, MPU, etc.

R_L : $\text{k}\Omega$

Voltage: V

Note: Connect a capacitor between IC pins 1 and 2 if V_{CC} line impedance is high.

2. Manual reset added

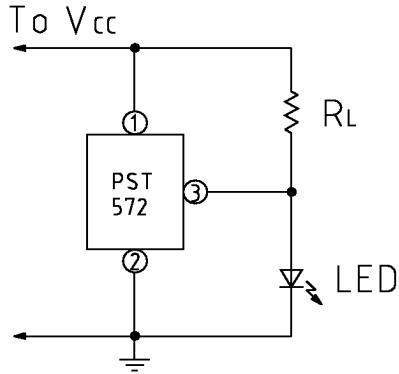


Note 1: Use R_L , C_L and R_m to prevent manual switch chattering. Note that R_m should be set to the following conditions.

$$R_m \leq 1/20R_L$$

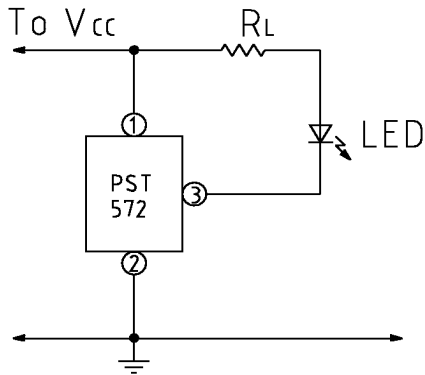
Note 2: Connect a capacitor between IC pins 1 and 2 if V_{CC} line impedance is high.

3. Battery checker (LED ON for high voltage)



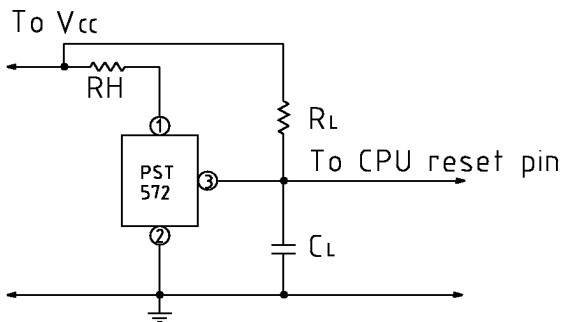
Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

4. Battery checker (LED ON for low voltage)



Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.

5. Hysteresis voltage UP method



When increasing hysteresis voltage for stable system operation, determine RH as follows and connect externally.

However, I_{ccH} is $-5000\text{PPM}/^\circ\text{C}$ so perform temperature compensation at RH when using over a wide temperature range.

Hysteresis voltage UP amount (ΔV_{sup}) is

$$\Delta V_{sup} \cong R_H \cdot I_{ccL}$$

Total hysteresis voltage (ΔV_{total}) is

$$\Delta V_{total} \cong V_s + \Delta V_{sup}$$

Note: Connect a capacitor between IC pins 1 and 2 if Vcc line impedance is high.