

# HD14541B

## Programmable Oscillator/Timer

The HD14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic. Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified  $V_{DD}$  range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency ( $f_{osc}$ ) with the  $n^{th}$  stage frequency being  $f_{osc}/2^n$ .

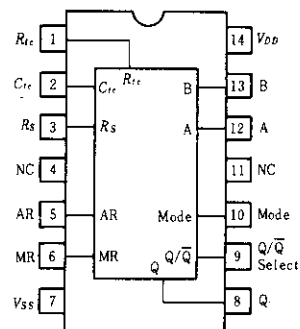
### FEATURES

- Available Outputs  $2^8$ ,  $2^{10}$ ,  $2^{13}$  or  $2^{16}$
- Increments on Positive Edge Clock Transitions
- Low Symmetrical Output Resistance (typically  $100\Omega @ 15V$ )
- Built-in Low Power RC Oscillator ( $\pm 2\%$  accuracy over temperature range and  $\pm 10\%$  supply and  $\pm 3\%$  over processing @  $< 10kHz$ )
- Oscillator Frequency Range = DC to 100kHz
- Oscillator May Be Bypassed if External Clock is Available (Apply external clock to Pin 3)
- Automatic Reset Initializes All Counters When Power Turns On (Limits- $V_{DD}$  from 8.5V to 18V when enabled)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as  $2^n$  Frequency Divider or Single Transition Timer
- Q/Q Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Supply Voltage Range = 3 to 18V

### MAXIMUM RATINGS (Voltages referenced to $V_{SS}$ )

Characteristic	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	$-0.5 \sim +18$	V
Input/Output Voltage	$V_{is}, V_{oH}$	$-0.5 \sim V_{DD} + 0.5$	V
DC Current Drain per Input Pin	$I_{in}$	$\pm 10$	mA
DC Current Drain per Output Pin	$I_{oL}, I_{oH}$	$\pm 45$	mA
Operating Temperature Range	$T_A$	$-40 \sim +85$	$^{\circ}C$
Storage Temperature Range	$T_{stg}$	$-65 \sim +150$	$^{\circ}C$
Power Dissipation	$P_d$	300	mW

### PIN ARRANGEMENT



(Top View)

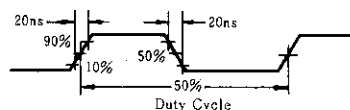
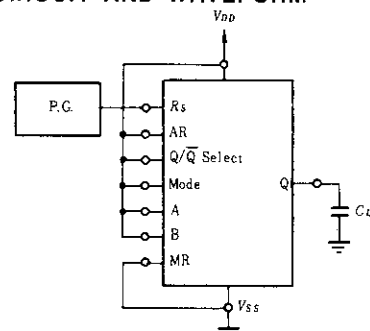
### TRUTH TABLE

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset ON
9	Output Initially Low After Reset	Output Initially High After Reset
10	Single Cycle Mode	Recycle Mode

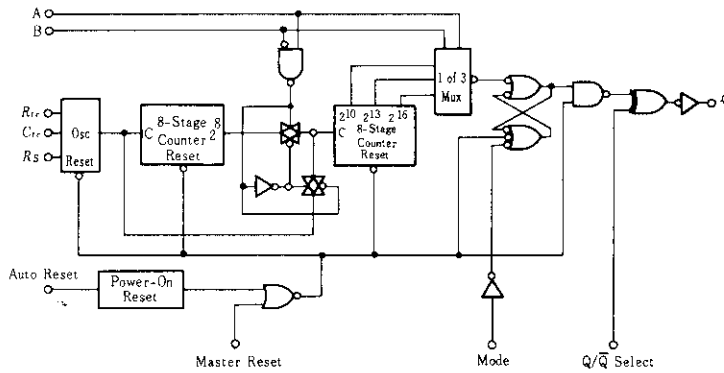
### FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages	Count $2^n$
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

### POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



■ BLOCK DIAGRAM



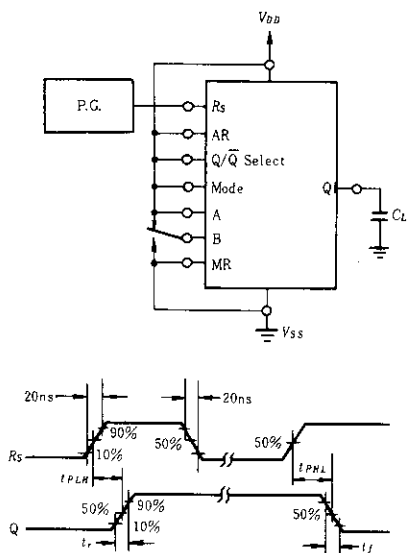
■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit		
			min	max	min	typ	max	min	max			
Output Voltage	V <sub>OL</sub>	5.0	V <sub>in</sub> = V <sub>DD</sub> or 0		—	0.05	—	0	0.05	—	0.05	V
		10			—	0.05	—	0	0.05	—	0.05	
		15			—	0.05	—	0	0.05	—	0.05	
	V <sub>OH</sub>	5.0	V <sub>in</sub> = 0 or V <sub>DD</sub>		4.95	—	4.95	5.0	—	4.95	—	V
		10			9.95	—	9.95	10	—	9.95	—	
		15			14.95	—	14.95	15	—	14.95	—	
Input Voltage	V <sub>IL</sub>	5.0	V <sub>out</sub> = 4.5 or 0.5 V		—	1.5	—	2.25	1.5	—	1.5	V
		10	V <sub>out</sub> = 9.0 or 1.0 V		—	3.0	—	4.50	3.0	—	3.0	
		15	V <sub>out</sub> = 13.5 or 1.5 V		—	4.0	—	6.75	4.0	—	4.0	
	V <sub>IH</sub>	5.0	V <sub>out</sub> = 0.5 or 4.5 V		3.5	—	3.5	2.75	—	3.5	—	V
		10	V <sub>out</sub> = 1.0 or 9.0 V		7.0	—	7.0	5.50	—	7.0	—	
		15	V <sub>out</sub> = 1.5 or 13.5 V		11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I <sub>OH</sub>	5.0	V <sub>OH</sub> = 2.5 V		-5.1	—	-4.27	-12.83	—	-3.5	—	mA
		10	V <sub>OH</sub> = 9.5 V		-2.69	—	-2.25	-6.75	—	-1.85	—	
		15	V <sub>OH</sub> = 13.5 V		-10.5	—	-8.8	-26.33	—	-7.22	—	
	I <sub>OL</sub>	5.0	V <sub>OL</sub> = 0.4 V		1.24	—	1.04	3.12	—	0.85	—	mA
		10	V <sub>OL</sub> = 0.5 V		3.18	—	2.66	8.0	—	2.18	—	
		15	V <sub>OL</sub> = 1.5 V		12.4	—	10.4	31.2	—	8.50	—	
Input Current	I <sub>in</sub>	15			—	±0.3	—	±0.0001	±0.3	—	±1.0	μA
Input Capacitance	C <sub>in</sub>		V <sub>in</sub> = 0		—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I <sub>DD</sub>	5.0	Zero Signal, per Package		—	20	—	0.005	20	—	150	μA
		10			—	40	—	0.010	40	—	300	
		15			—	80	—	0.015	80	—	600	
Auto Reset Quiescent Current	I <sub>DDR</sub>	5.0	Pin 5 is low		—	200	—	7	200	—	1200	μA
		10			—	250	—	30	250	—	1500	
		15			—	500	—	82	500	—	2000	
Total Supply Current*	I <sub>T</sub>	5.0	Dynamic + I <sub>DD</sub> , per Gate		—	—	—	0.4	—	—	—	μA
		10			—	—	—	0.8	—	—	—	
		15	C <sub>L</sub> = 50pF, f = 1kHz		—	—	—	1.2	—	—	—	

\* To calculate total supply current at frequency other than 1kHz.

@V<sub>DD</sub> = 5.0V I<sub>T</sub> = (0.4 μA/kHz)f + I<sub>DD</sub>, @V<sub>DD</sub> = 10V I<sub>T</sub> = (0.8 μA/kHz)f + I<sub>DD</sub>, @V<sub>DD</sub> = 15V I<sub>T</sub> = (1.2 μA/kHz)f + I<sub>DD</sub>

■ SWITCHING TIME TEST CIRCUIT



■ SWITCHING CHARACTERISTICS ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

Characteristic		Symbol	$V_{DD}(V)$	min	typ	max	Unit
Output Rise Time		$t_r$	5.0	—	180	400	ns
			10	—	90	200	
			15	—	65	160	
Output Fall Time		$t_f$	5.0	—	100	200	ns
			10	—	50	100	
			15	—	37	80	
Propagation Delay Time	Clock to Q ( $2^8$ Output)	$t_{PLH}$	5.0	—	3.5	10.5	$\mu\text{s}$
			10	—	1.25	3.8	
			15	—	0.9	2.9	
	Clock to Q ( $2^{16}$ Output)	$t_{PHL}$	5.0	—	6.0	18	
			10	—	3.5	10	
			15	—	2.5	7.5	
Clock Pulse Width		$PW_C$	5.0	900	300	—	ns
			10	300	100	—	
			15	225	85	—	
Clock Frequency		$PRF$	5.0	—	1.5	—	MHz
			10	—	4.0	—	
			15	—	6.0	—	
Minimum Master Reset Pulse Width		$PW_{MR}$	5.0	900	300	—	ns
			10	300	100	—	
			15	225	85	—	



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

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