

# HD14076B

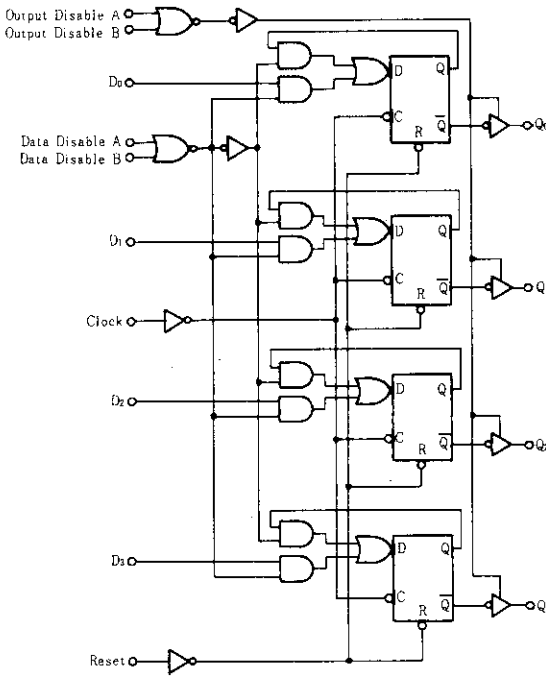
## 4-bit D-type Register

The HD14076B 4-bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

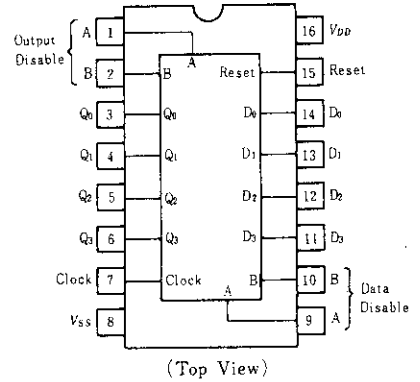
### ■ FEATURES

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- For Bus Buffer Registers
- Quiescent Current = 5nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

### ■ LOGIC DIAGRAM



### ■ PIN ARRANGEMENT



### ■ TRUTH TABLE

Reset	Clock	Inputs			Output
		Data Disable		Data	
		A	B	D	Q
1	×	×	×	×	0
0	0	×	×	×	Q <sub>n</sub>
0		1	×	×	Q <sub>n</sub>
0		×	1	×	Q <sub>n</sub>
0		0	0	0	0
0		0	0	1	1

Note) × = Don't Care

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

**ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit	
			min	max	min	typ	max	min	max		
Output Voltage	$V_{OL}$	$V_{DD} = 5.0$	$V_{in} = V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
		10		—	0.05	—	0	0.05	—	0.05	
		15		—	0.05	—	0	0.05	—	0.05	
	$V_{OH}$	$V_{DD} = 5.0$	$V_{in} = 0$ or $V_{DD}$	4.95	—	4.95	5.0	—	4.95	—	V
		10		9.95	—	9.95	10	—	9.95	—	
		15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	$V_{IL}$	$V_{out} = 4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V	
		$V_{out} = 9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0		
		$V_{out} = 13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0		
	$V_{IH}$	$V_{out} = 0.5$ or $4.5V$	3.5	—	3.5	2.75	—	3.5	—	V	
		$V_{out} = 1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—		
		$V_{out} = 1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—		
Output Drive Current	$I_{OH}$	$V_{OH} = 2.5V$	-1.0	—	-0.8	-1.7	—	-0.6	—	mA	
		$V_{OH} = 4.6V$	-0.2	—	-0.16	-0.36	—	-0.12	—		
		$V_{OH} = 9.5V$	-0.5	—	-0.4	-0.9	—	-0.3	—		
		$V_{OH} = 13.5V$	-1.4	—	-1.2	-3.5	—	-1.0	—		
	$I_{OL}$	$V_{OL} = 0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA	
		$V_{OL} = 0.5V$	1.3	—	1.1	2.25	—	0.9	—		
$V_{OL} = 1.5V$		3.6	—	3.0	8.8	—	2.4	—			
Input Current	$I_{in}$	15	—	$\pm 0.3$	—	$\pm 0.0001$	$\pm 0.3$	—	$\pm 0.0$	$\mu A$	
Input Capacitance	$C_{in}$		$V_{in} = 0$	—	—	—	5.0	7.5	—	pF	
Quiescent Current	$I_{DD}$	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	$\mu A$
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	$I_T$	5.0	Dynamic + $I_{DD}$ , per Gate, $C_L = 50pF$ $f = 1kHz$	—	—	—	0.75	—	—	—	$\mu A$
		10		—	—	—	1.50	—	—	—	
		15		—	—	—	2.25	—	—	—	

\* To calculate total supply current at frequency other than 1kHz.

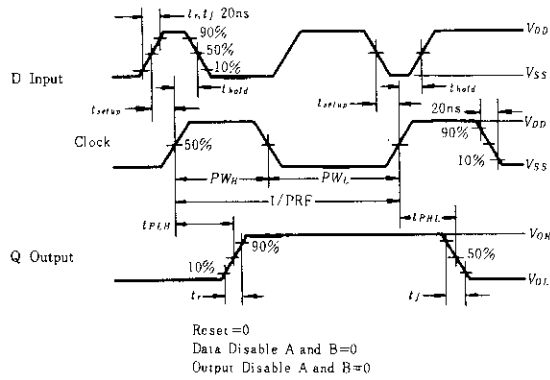
@ $V_{DD} = 5.0V$   $I_T = (0.75 \mu A/kHz)f + I_{DD}$ , @ $V_{DD} = 10V$   $I_T = (1.50 \mu A/kHz)f + I_{DD}$ , @ $V_{DD} = 15V$   $I_T = (2.25 \mu A/kHz)f + I_{DD}$

**SWITCHING CHARACTERISTICS** ( $C_L = 50\text{pF}$ ,  $T_a = 25^\circ\text{C}$ )

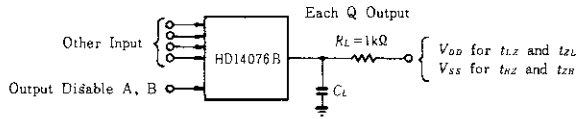
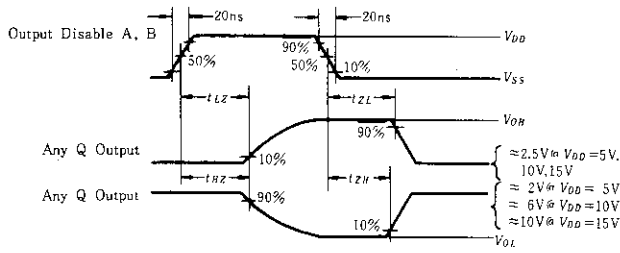
Characteristic		Symbol	$V_{DD}$ (V)	min	typ	max	Unit
Output Rise Time		$t_r$	5.0	—	180	360	ns
			10	—	90	180	
			15	—	65	130	
Output Fall Time		$t_f$	5.0	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation Delay Time	Clock	$t_{PLH}$ , $t_{PHL}$	5.0	—	300	600	ns
			10	—	125	250	
			15	—	90	180	
	Reset	5.0	—	300	600		
		10	—	125	250		
		15	—	90	180		
Output Disable Time		$t_{HZ}$ , $t_{LZ}$	5.0	—	150	300	ns
			10	—	60	120	
			15	—	45	90	
Output Enable Time		$t_{ZH}$ , $t_{ZL}$	5.0	—	200	400	ns
			10	—	80	160	
			15	—	60	120	
Clock Pulse Width		$PW_C$	5.0	260	130	—	ns
			10	110	55	—	
			15	80	40	—	
Reset Pulse Width		$PW_R$	5.0	370	185	—	ns
			10	150	75	—	
			15	110	55	—	
Setup Time		$t_{setup}$	5.0	30	15	—	ns
			10	10	5	—	
			15	4	2	—	
Hold Time		$t_{hold}$	5.0	130	65	—	ns
			10	60	30	—	
			15	50	25	—	
Data Disable Setup Time		$t_{setup}$	5.0	220	110	—	ns
			10	80	40	—	
			15	50	25	—	
Clock Pulse Rise and Fall Time		$t_r$ , $t_f$	5.0	—	—	15	$\mu\text{s}$
			10	—	—	15	
			15	—	—	15	
Clock Frequency		$PRF$	5.0	—	3.6	1.8	MHz
			10	—	9.0	4.5	
			15	—	12	6.0	

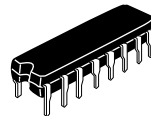
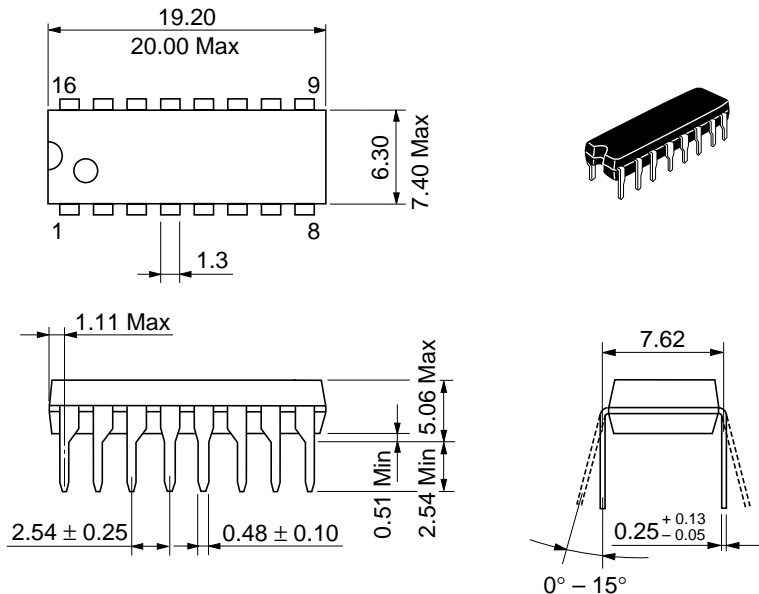
■ DYNAMIC SIGNAL WAVEFORMS

● TIMING DIAGRAM



● Three-state Enable/Disable Delay





Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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