

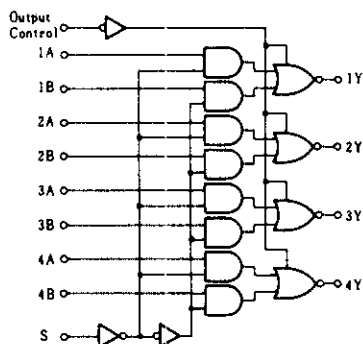
HD74LS258

● Quadruple 2-line-to-1-line Data Selectors/Multiplexers
(with three-state outputs)

This multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

■ BLOCK DIAGRAM



■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Output current	I_{OH}	—	—	-2.6	mA
	I_{OL}	—	—	8	mA

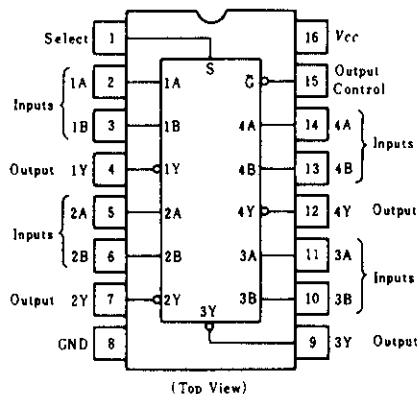
■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item		Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage		V_{IH}		2.0	—	—	V	
		V_{IL}		—	—	0.8	V	
Output voltage		V_{OH}	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -2.6\text{mA}$	2.4	—	—	V	
		V_{OL}	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}$	$I_{OL} = 4\text{mA}$	—	—	0.4	V
				$I_{OL} = 8\text{mA}$	—	—	0.5	V
Output current		I_{OZH}	$V_{CC} = 5.25\text{V}, V_{IH} = 2\text{V}, V_O = 2.4\text{V}$	—	—	20	μA	
		I_{OZL}	$V_{CC} = 5.25\text{V}, V_{IH} = 2\text{V}, V_O = 0.4\text{V}$	—	—	-20	μA	
Input current	S	I_{IH}	$V_{CC} = 5.25\text{V}, V_i = 2.7\text{V}$	—	—	40	μA	
	except S			—	—	20	μA	
	S	I_{IL}	$V_{CC} = 5.25\text{V}, V_i = 0.4\text{V}$	—	—	-0.8	mA	
	except S			—	—	-0.4	mA	
	S	I_i	$V_{CC} = 5.25\text{V}, V_i = 7\text{V}$	—	—	0.2	mA	
	except S			—	—	0.1	mA	
Short-circuit output current		I_{OS}	$V_{CC} = 5.25\text{V}$	-30	—	-130	mA	
Supply current	All outputs high	I_{CC}	$V_{CC} = 5.25\text{V}$	—	—	7	mA	
	All outputs low			—	—	11	mA	
	All outputs off			—	—	12	mA	
Input clamp voltage		V_{IK}	$V_{CC} = 4.75\text{V}, I_{IN} = -18\text{mA}$	—	—	-1.5	V	

* $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$

** I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

■ PIN ARRANGEMENT



■ FUNCTION TABLE

OC	Input			Output
	S	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note) H; high level, L; low level, X; irrelevant
Z; off (high-impedance) state of a 3-state output

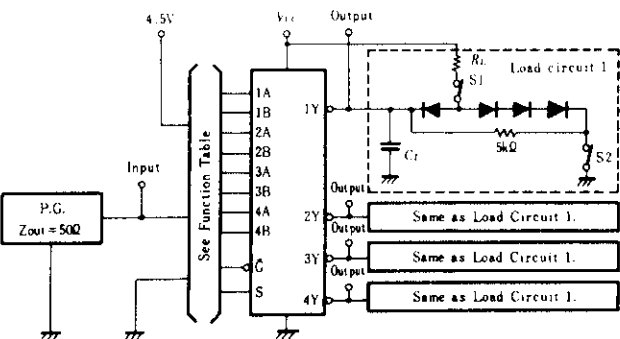
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SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$)

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	A, B	Y	$R_l = 2k\Omega$ $C_l = 15pF$	—	12	18	ns
	t_{PHL}				—	12	18	ns
	t_{PLH}	S	Y		—	14	21	ns
	t_{PHL}				—	14	21	ns
Output enable time	t_{ZN}	OUTPUT CONTROL	Y		—	20	30	ns
	t_{ZL}	CONTROL			—	20	30	ns
Output disable time	t_{NZ}	OUTPUT CONTROL	Y	$R_l = 2k\Omega$ $C_l = 5pF$	—	18	30	ns
	t_{LZ}	CONTROL			—	16	25	ns

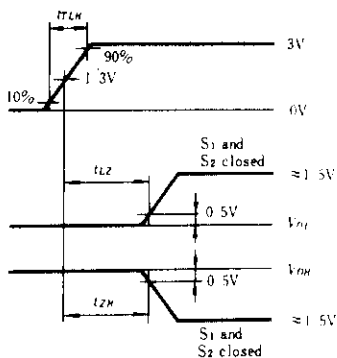
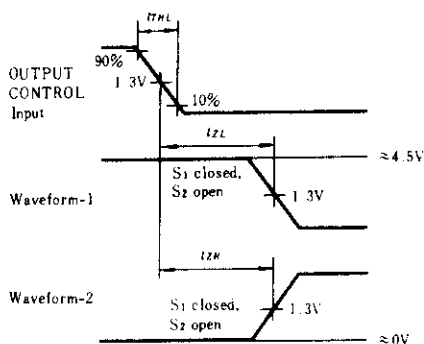
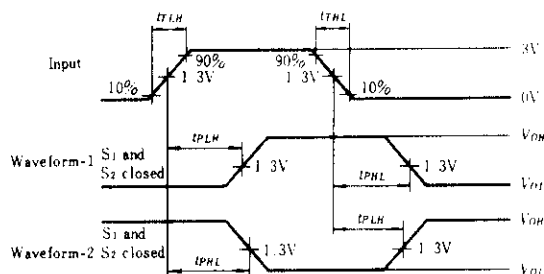
TESTING METHOD

1) Test Circuit

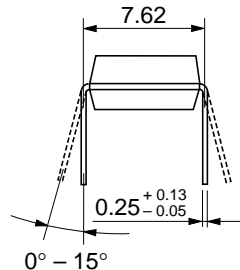
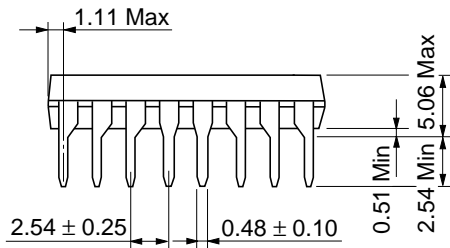
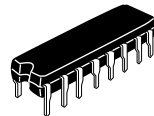
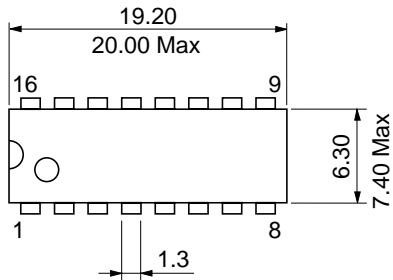


- Notes
- C_L includes probe and jig capacitance.
 - All diodes are 1S2074 (H).

Waveform



- Notes
- Input pulse: $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, $PRR=1MHz$, duty cycle=50%
 - Waveform-1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 - Waveform-2 is for an output with internal conditions such that the output is high except when disabled by the output control.

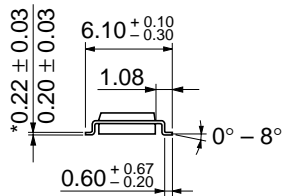
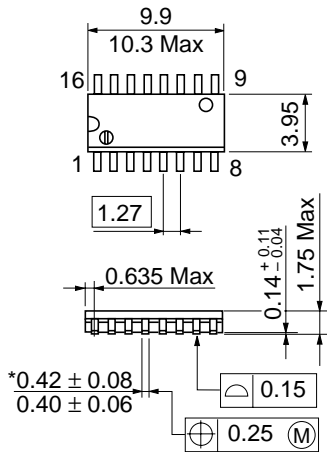


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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